Nisshinbo Micro Devices Inc.

Industrial NV3601

CMOS Output Window Voltage Detector with High Withstand of SENSE Pin

FEATURES

- Input Voltage Range (Maximum Rating): 2.4 V to 6.0 V (7.0 V)
- SENSE Pin Voltage Range (Maximum Rating): 0 V to 42.0 V (50.0 V)
- Operating Temperature Range: -40 °C to 125 °C
- Quiescent Current: Typ. 1.4 μA (VDD pin only), Max. 4.0 μA (Includes SENSE pin current)
- Under Voltage Detection: 3.3 V to 19.8 V (0.1 V increment)
  Accuracy: ±0.6 % (T_a = 25 °C), ±1.5 % (-40 °C to 125 °C)
- Over Voltage Detection: 4.5 V to 22.2 V (0.1 V increment)
  Accuracy: ±0.6 % (T_a = 25 °C), ±1.5 % (-40 °C to 125 °C)
- Hysteresis: A/C/E/G Typ. 1.0% with hysteresis; B/D/F/H No hysteresis
- Under Voltage/Over Voltage Detection Delay Time: Typ. 40 μs
- Under Voltage/Over Voltage Release Delay Time: Typ. 230 μs
- Output Type: NMOS Open Drain or CMOS

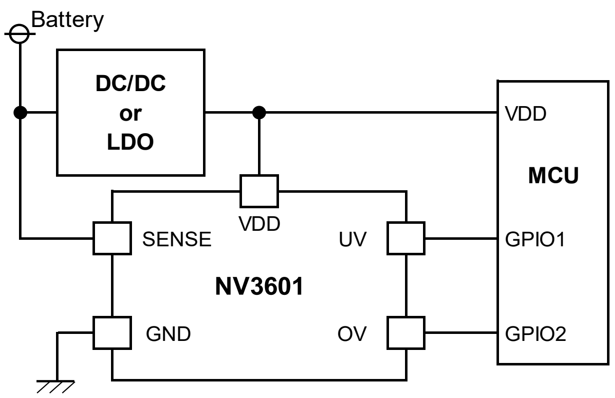
GENERAL DESCRIPTION

The NV3601 is using a CMOS based window voltage detector.
In addition to monitoring voltage drops, it can also detect over voltages as abnormalities, allowing you to understand the operating status of your system in detail.
Additionally, the high withstand voltage of 42 V at the SENSE pin allows this device to directly monitor battery voltage.
NMOS open drain output type or CMOS output type can be selected for the output type.
Therefore, external voltage divider resistors and pull-up resistors are no longer required, reducing the number of external components and the dark current of the system.
Furthermore, the presence or absence of hysteresis and the detection output logic ("Low" or "High") can be selected, allowing optimal operation to be achieved according to the system functions.
This product (-D) is a highly reliable product that has undergone high temperature tests and reliability tests that are more severe than consumer products.

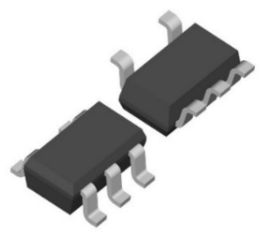
APPLICATIONS

- Power supply voltage supervisor for Factory Automation Equipment.
- Voltage supervisor of control devices like a PLCs.

TYPICAL APPLICATION CIRCUIT



PACKAGE



SOT-23-5-DC
2.9 × 2.8 × 1.1
(UNIT : mm)

PRODUCT NAME INFORMATION

NV3601 aa bbb c dd e

Description of configuration

Composition	Item	Description
aa	Package Code	DC: SOT-23-5-DC
bbb	Setting Voltage	Set under voltage detection (V_{UVDET}) and over voltage detection (V_{OVDET}) The under voltage detection can be set between 3.3 V to 19.8 V (0.1 V increment), The over voltage detection can be set between 4.5 V to 22.2 V (0.1 V increment).
c	Version	Output type ("NMOS open drain" or "CMOS"), Output logic when detecting ("Low" or "High"), Hysteresis ("With hysteresis" or "No hysteresis")
dd	Packing	Insert direction. Refer to the packing specifications.
e	Grade	Indicates the quality grade. D: Industrial

Version

c	Output Type	Output Logic at Detection	Hysteresis
A	NMOS open drain	Low	✓
B	NMOS open drain	Low	-
C	NMOS open drain	High	✓
D	NMOS open drain	High	-
E	CMOS	Low	✓
F	CMOS	Low	-
G	CMOS	High	✓
H	CMOS	High	-

Grade

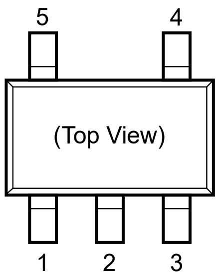
e	Applications	Operating Temperature Range	Test Temperature
D	Industrial equipment and Social infrastructures	-40 °C to 125 °C	25 °C, 125 °C

ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY PER REEL (pcs/reel)
NV3601 DC bbb c E1 D	SOT-23-5-DC	Yes	Yes	Sn	14.0	3000

Click here for checking details.
Note: Contact our sales representatives for other voltages.

PIN DESCRIPTIONS

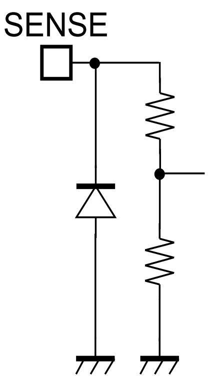


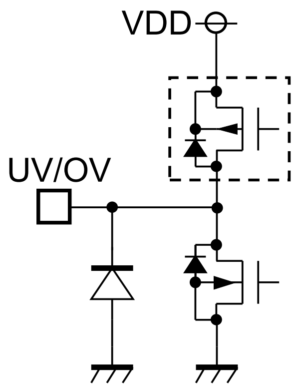
SOT-23-5-DC Pin Configuration

Pin No.	Pin Name	I/O	Description
1	SENSE	I	SENSE Voltage Input Pin
2	GND	-	Ground Pin
3	UV	O	Under Voltage Detection Output Pin NV3601DCxxxA/B/E/F: outputs "Low" reset signal when a voltage drops below the detection voltage. NV3601DCxxxC/D/G/H: outputs "High" reset signal when a voltage drops below the detection voltage. The "High" output level for CMOS output type is the VDD pin voltage.
4	OV	O	Over Voltage Detection Output Pin NV3601DCxxxA/B/E/F: outputs "Low" reset signal when a voltage drops below the detection voltage. NV3601DCxxxC/D/G/H: outputs "High" reset signal when a voltage drops below the detection voltage. The "High" output level for CMOS output type is the VDD pin voltage.
5	VDD	Power	Power Supply Input Pin

Please refer to "*TYPICAL APPLICATION CIRCUIT*" or "*THEORY OF OPERATION*" for details.

Internal Equivalent Circuit Diagram of Pin





※Dotted frame corresponds to (NV3601DCxxxE/F/G/H)

SENSE pin internal equivalent circuit diagram

UV pin / OV pin internal equivalent circuit diagram

ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
VDD Pin Voltage	V_{DD}	-0.3 to 7.0	V
SENSE Pin Voltage	V_{SENSE}	-0.3 to 50.0	V
UV Pin Voltage	V_{UVOUT}	-0.3 to 7.0	V
OV Pin Voltage	V_{OVOUT}	-0.3 to 7.0	V
UV Pin Output Current	I_{UVOUT}	30	mA
OV Pin Output Current	I_{OVOUT}	30	mA
Junction Temperature Range [*1]	T_j	-40 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

[*1] Calculate the power consumption of the IC from the operating conditions and calculate the junction temperature with the thermal resistance. Please refer to "*THERMAL CHARACTERISTICS*" for the thermal resistance under our measurement board conditions.

THERMAL CHARACTERISTICS

Parameter	Measurement Result	Unit
Thermal Resistance (θja)	150	°C/W
Thermal Characterization Parameter (ψjt)	51	

θja : Junction-to-Ambient Thermal Resistance
ψjt : Junction-to-Top Thermal Characterization Parameter

For more information, click *here*.

ELECTROSTATIC DISCHARGE RATINGS

	Conditions	Protection Voltage
HBM	C = 100 pF, R = 1.5 kΩ	±2000 V
CDM		±1000 V

ELECTROSTATIC DISCHARGE RATINGS

The electrostatic discharge test is done based on JESD47.
In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

RECOMMENDED OPERATING CONDITIONS

	Symbol	Ratings	Unit
VDD Pin Voltage	V_{DD}	2.4 to 6.0	V
SENSE Pin Voltage	V_{SENSE}	0 to 42.0	V
UV Pin Pull-up Voltage (NV3601DCxxxA/B/C/D)	V_{UVUP}	0 to 6.0	V
OV Pin Pull-up Voltage (NV3601DCxxxA/B/C/D)	V_{OVUP}	0 to 6.0	V
Operating Temperature Range	T_a	-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{DD} = 6 V unless otherwise specified.
For NV3601DCxxxA/B/C/D (NMOS Open Drain Type), pull-up resistor (R_{UP}) = 100 kΩ, pull-up voltage (V_{UVUP}, V_{OVUP}) = 5 V.
For parameter that do not describe the temperature condition, the MIN/MAX value under the condition of -40 °C ≤ Ta ≤ 125 °C is described.

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Under Voltage Detection	V_{UVDET}	V_{SENSE} = Falling	T_a = 25 °C	×0.994	-	×1.006	V
			-40 °C ≤ T_a ≤ 125 °C	×0.985	-	×1.015	V
Over Voltage Detection	V_{OVDET}	V_{SENSE} = Rising	T_a = 25 °C	×0.994	-	×1.006	V
			-40 °C ≤ T_a ≤ 125 °C	×0.985	-	×1.015	V
Under Voltage Threshold Hysteresis	V_{UVHYS}	With hysteresis (NV3601DCxxxA/C/E/G)		0.5	1.0	1.5	%
		No hysteresis (NV3601DCxxxB/D/F/H)		-15	-	15	mV
Over Voltage Threshold Hysteresis	V_{OVHYS}	With hysteresis (NV3601DCxxxA/C/E/G)		0.5	1.0	1.5	%
		No hysteresis (NV3601DCxxxB/D/F/H)		-15	-	15	mV
Quiescent Current *1	I_Q	V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2		-	1.4	2.7	μA
SENSE Pin Current	I_{SENSE}	V_{SENSE} = 12 V		0.2	-	1.3	μA
UVLO Detection Voltage *2	$V_{UVLODET}$	V_{DD} = Falling		2.1	-	2.3	V
UVLO Release Voltage *2	$V_{UVLOREL}$	V_{DD} = Rising		2.2	-	2.4	V
UV Pin Minimum Operating Voltage *3	V_{DDLUV}			-	-	1.7	V
OV Pin Minimum Operating Voltage *3	V_{DDLOV}			-	-	1.7	V
UV Pin Output Current	I_{UVOUT}	UV = "High", V_{DD} = 2.4 V (NV3601DCxxxE/F/G/H)	V_{UVOUT} = V_{DD} - 0.1 V	0.10	-	-	mA
			V_{UVOUT} = V_{DD} - 0.3 V	0.25	-	-	
		UV = "Low", V_{DD} = 2.4 V	V_{UVOUT} = 0.1 V	0.40	-	-	mA
			V_{UVOUT} = 0.3 V	1.00	-	-	
OV Pin Output Current	I_{OVOUT}	OV = "High", V_{DD} = 2.4 V (NV3601DCxxxE/F/G/H)	V_{OVOUT} = V_{DD} - 0.1 V	0.10	-	-	mA
			V_{OVOUT} = V_{DD} - 0.3 V	0.25	-	-	
		OV = "Low", V_{DD} = 2.4 V	V_{OVOUT} = 0.1 V	0.40	-	-	mA
			V_{OVOUT} = 0.3 V	1.00	-	-	
UV Pin Leakage Current *4	$I_{UVOUTLEAK}$	V_{UVOUT} = 6 V (NV3601DCxxxA/B/C/D)		-	-	0.3	μA
OV Pin Leakage Current *4	$I_{OVOUTLEAK}$	V_{OVOUT} = 6 V (NV3601DCxxxA/B/C/D)		-	-	0.3	μA
Under Voltage Detection Delay Time *5	t_{UVDET}	V_{DD} = 2.4 V		-	40	90	μs
Over Voltage Detection Delay Time *5	t_{OVDET}	V_{DD} = 2.4 V		-	40	90	μs
Under Voltage Release Delay Time *5	t_{UVREL}			-	230	600	μs
Over Voltage Release Delay Time *5	t_{OVREL}			-	230	600	μs

All test items listed in Electrical Characteristics are done under the pulse load condition (T_j ≈ T_a = 25 °C/125 °C)

*1 VDD pin current.
*2 Due to circuit configuration, $V_{UVLODET}$ ≥ $V_{UVLOREL}$ does not hold. The hysteresis is Typ. 0.09 V.
*3 This minimum VDD voltage to prevent UV/OV pin output from becoming indefinite.
Judgment conditions are as follows.
NV3601DCxxxA/B/E/F ("Low" output at detection): V_{UVOUT} ≤ 0.1 V, V_{OVOUT} ≤ 0.1 V
NV3601DCxxxC/D ("High" output at detection, NMOS open drain): V_{UVOUT} ≥ V_{UVUP} - 0.1 V, V_{OVOUT} ≥ V_{OVUP} - 0.1 V
NV3601DCxxxG/H ("High" output at detection, CMOS): V_{UVOUT} ≥ V_{DD} - 0.1 V, V_{OVOUT} ≥ V_{DD} - 0.1 V
*4 Leakage current when the NMOS output transistor is OFF.
*5 For detailed conditions of the delay time, refer to "*THEORY OF OPERATION*".

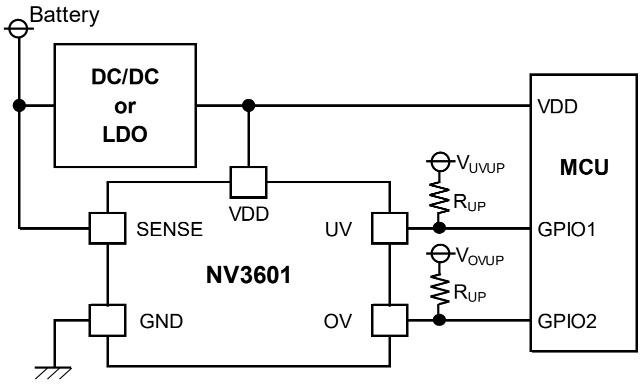
ELECTRICAL CHARACTERISTICS

[Unit: V]

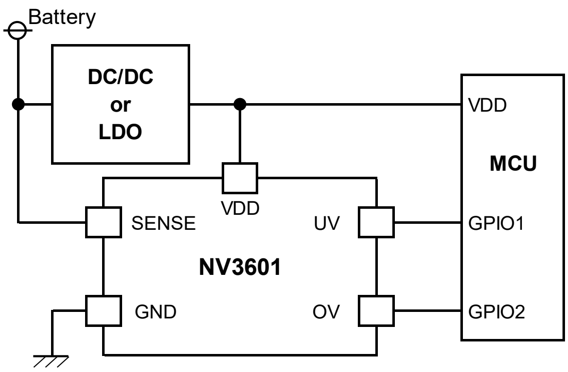
PRODUCT NAME	V_{UVDET}					V_{OVDET}				
	T_a = 25 °C			-40 °C ≤ T_a ≤ 125 °C		T_a = 25 °C			-40 °C ≤ T_a ≤ 125 °C	
	MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX
NV3601DC001 xxxx	3.280	3.3	3.320	3.250	3.350	4.473	4.5	4.527	4.432	4.568
NV3601DC002 xxxx	19.681	19.8	19.919	19.503	20.097	22.066	22.2	22.334	21.867	22.533
NV3601DC003 xxxx	8.946	9.0	9.054	8.865	9.135	19.581	19.7	19.819	19.404	19.996
NV3601DC004 xxxx	4.473	4.5	4.527	4.432	4.568	18.190	18.3	18.410	18.025	18.575
NV3601DC005 xxxx	5.665	5.7	5.735	5.614	5.786	18.090	18.2	18.310	17.927	18.473
NV3601DC006 xxxx	8.449	8.5	8.551	8.372	8.628	18.389	18.5	18.611	18.222	18.778
NV3601DC007 xxxx	4.970	5.0	5.030	4.925	5.075	18.886	19.0	19.114	18.715	19.285
NV3601DC008 xxxx	9.641	9.7	9.759	9.554	9.846	19.383	19.5	19.617	19.207	19.793
NV3601DC009 xxxx	8.449	8.5	8.551	8.372	8.628	19.383	19.5	19.617	19.207	19.793

All test items listed in Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a$ = 25 °C/125 °C)

TYPICAL APPLICATION CIRCUIT



NV3601DCxxxA/B/C/D



NV3601DCxxxE/F/G/H

EXTERMAL COMPONENTS

Pull-up Resistor (R_{UP})

NV3601DCxxxA/B/C/D: UV pin voltage and OV pin voltage depend on the external pull-up resistor (R_{UP}).
Refer to the next formula and choose an appropriate value for the resistance.
Herein, V_{UP} is pull-up voltage, $I_{OUTLEAK}$ is the leakage current while NMOS output transistor turns off.

(1) Lower limit of the pull-up resistor (R_{UP})
"Low" voltage level (V_{OUTL}) of UV/OV is determined by on resistance (R_{ON}) of NMOS output transistor, pull-up resistor (R_{UP}) and pull-up voltage (V_{UP}).

$$V_{OUTL} = R_{ON} / (R_{ON} + R_{UP}) \times V_{UP}$$

The maximum value of R_{ON} can be calculated by the next equation with using the value of "UV/OV Pin Output Current" of Electrical Characteristics Table. ($V_{OUTL} \leq 0.3$ V)

$$R_{ON}\ (MAX) = 0.3\ V / 1\ mA = 0.3\ k\Omega$$

To obtain the desirable "Low" voltage level, the minimum value of R_{UP} should satisfy the next equation.

$$R_{UP} \geq (V_{UP} - V_{OUTL}) / V_{OUTL} \times R_{ON}$$

* If R_{UP} is small, the quiescent current under the condition of "Low" output ($\approx V_{UP}/R_{UP}$) may increase.
(The recommendation value of the pull-up resistor is 1 kΩ or more.)

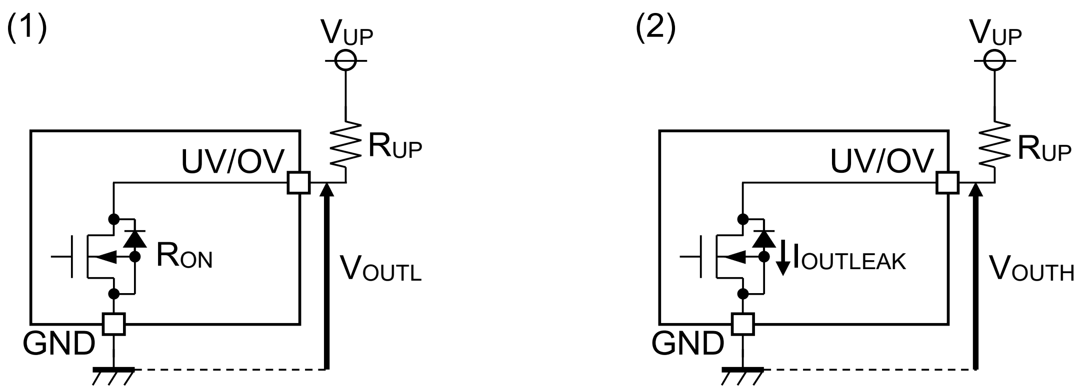
(2) Higher limit of the pull-up resistor (R_{UP})
"High" voltage level (V_{OUTH}) of UV/OV is determined by the leakage current ($I_{OUTLEAK}$), pull-up resistor (R_{UP}) and pull-up voltage (V_{UP}).

$$V_{OUTH} = V_{UP} - I_{OUTLEAK} \times R_{UP}$$

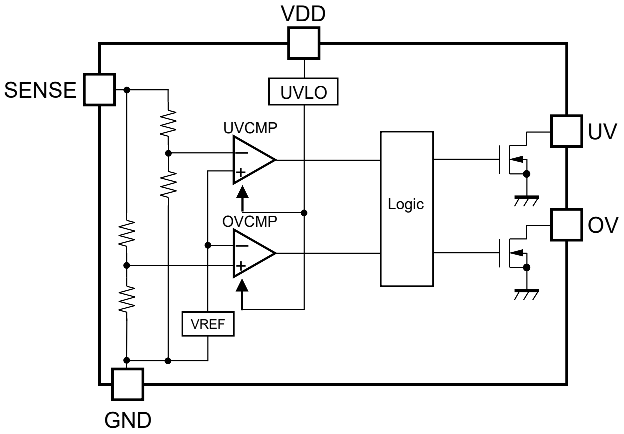
The maximum value of $I_{OUTLEAK}$ is specified in the Electrical Characteristics Table. (UV/OV pin leakage current = 0.3 μA.)
To satisfy the desirable "High" voltage, the higher limit of R_{UP} should satisfy the next equation.

$$R_{UP} \leq (V_{UP} - V_{OUTH}) / I_{OUTLEAK}$$

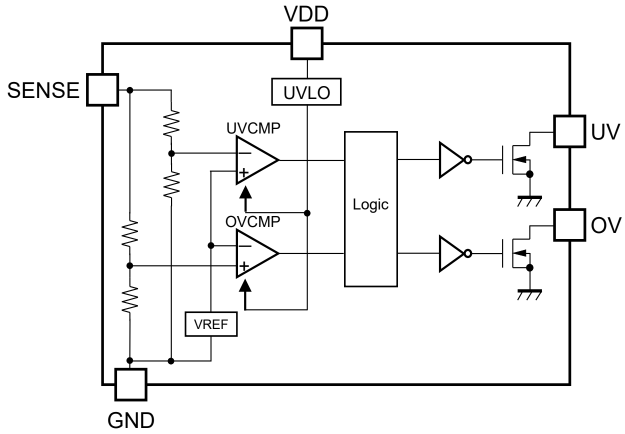
(Ex.)
V_{UP} = 5 V, The target UV/OV pin voltage "Low" = 0.3 V, "High" = 4.7 V
By the equation (1), $R_{UP} \geq (5\ V - 0.3\ V) / 0.3\ V \times 0.3\ k\Omega = 4.7\ k\Omega$
By the equation (2), $R_{UP} \leq (5\ V - 4.7\ V) / 0.3\ \mu A = 1\ M\Omega$
Therefore, appropriate value range of pull-up resistor is from 4.7 kΩ to 1 MΩ.



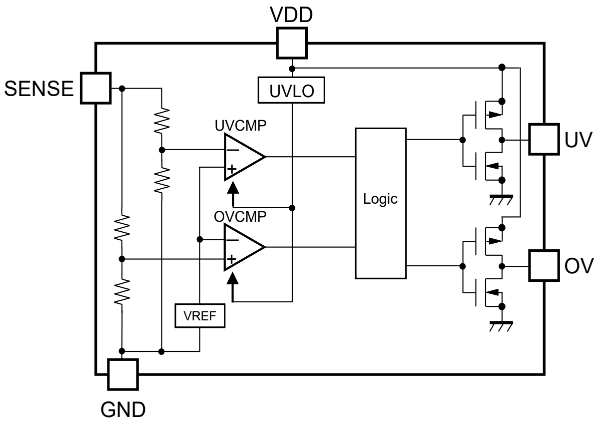
BLOCK DIAGRAMS



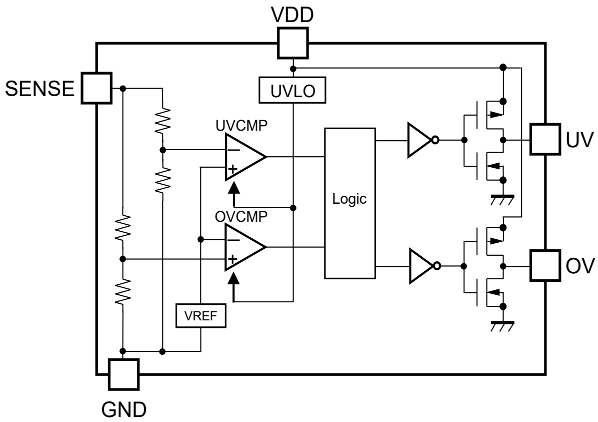
NV3601DCxxxA/B Block Diagram



NV3601DCxxxC/D Block Diagram



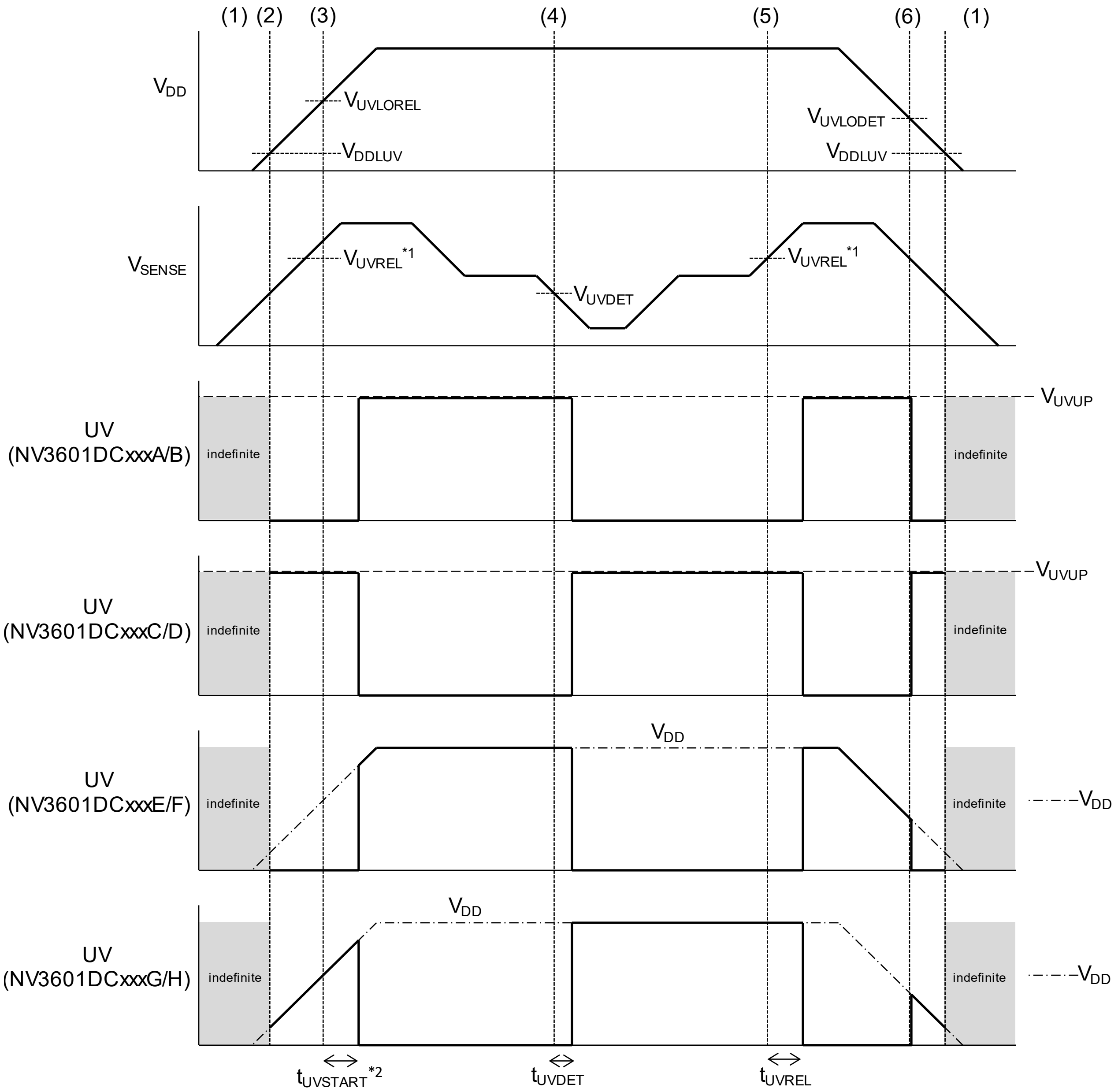
NV3601DCxxxE/F Block Diagram



NV3601DCxxxG/H Block Diagram

THEORY OF OPERATION

1. During VDD pin power-up, when V_{DD} exceeds the UVLO release voltage, if $V_{SENSE} \geq V_{UVREL}$



(1) V_{DD} is equal or lower than UV pin minimum operating voltage (V_{DDLUV}), UV output is not guaranteed. "(Indefinite)"

(2) V_{DD} exceeds V_{DDLUV}, UV output asserts "detected condition".

(3) V_{DD} exceeds UVLO release voltage ($V_{UVLOREL}$), if SENSE pin voltage (V_{SENSE}) is equal or more than the UV release voltage[*1] ($V_{UVREL} = V_{UVDET} + V_{UVHYS}$), after the UV start-up time[*2] ($t_{UVSTART}$: Max. 1 ms), UV output asserts "released condition". Even though V_{SENSE} falls, unless otherwise the voltage is less than the UV detection voltage (V_{UVDET}), "released condition" is maintained.

(4) Further V_{SENSE} falls and be lower than the V_{UVDET}, after the UV detection delay time (t_{UVDET}: Typ. 40 μs), UV output asserts "detected condition".

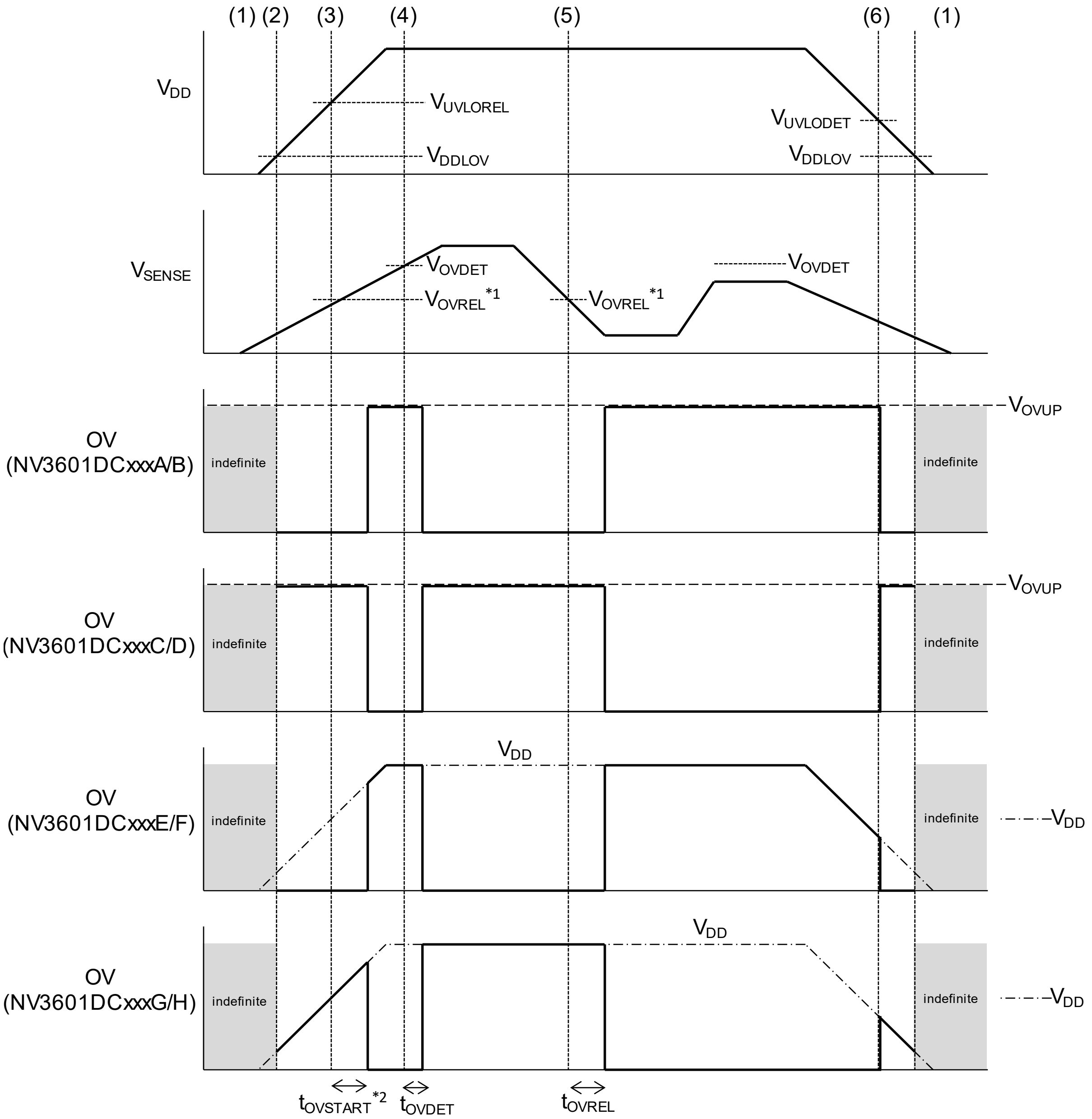
(5) V_{SENSE} rises and exceeds V_{UVREL}, after the UV release delay time (t_{UVREL}: Typ. 230 μs), UV output asserts "released condition".

(6) V_{DD} falls and when it becomes equal or lower than the UVLO detection voltage ($V_{UVLODET}$), UV output asserts "detected condition".

[*1] In NV3601DCxxxB/D/F/H, $V_{UVREL}=V_{UVDET}$.

[*2] UV start-up time ($t_{UVSTART}$) is the sum of UVLO release delay time and UV release delay time.

2. During VDD pin power-up, when V_{DD} exceeds the UVLO release voltage, if $V_{SENSE} \leq V_{OVREL}$



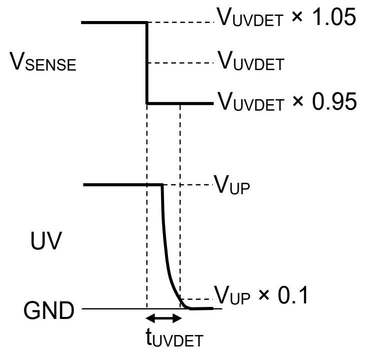
(1) V_{DD} is equal or lower than OV pin minimum operating voltage (V_{DDLOV}), OV output is not guaranteed. "(Indefinite)".
(2) V_{DD} exceeds V_{DDLOV}, OV output asserts " detected condition".
(3) V_{DD} exceeds UVLO release voltage ($V_{UVLOREL}$), if SENSE pin voltage (V_{SENSE}) is equal or lower than the OV release voltage[*1] ($V_{OVREL} = V_{OVDET} - V_{OVHYS}$), after OV start-up time[*2] ($t_{OVSTART}$: Max. 1 ms), OV output asserts "released condition".
(4) Further V_{SENSE} rises, and when it becomes equal or more than OV detection voltage (V_{OVDET}), after OV detection delay time (t_{OVDET}: Typ. 40 µs), OV output asserts "detected condition".
(5) V_{SENSE} falls and when it becomes equal or lower than V_{OVREL}, after OV release delay time (t_{OVREL}: Typ. 230 µs), OV output asserts "released condition". Even though V_{SENSE} rises, unless otherwise the voltage is more than V_{OVDET}, "released condition" is maintained.
(6) V_{DD} falls and when it becomes equal or less than UVLO detection voltage ($V_{UVLODET}$), OV output asserts "detected condition".

[*1] In NV3601DCxxxB/D/F/H, V_{OVREL}=V_{OVDET}.

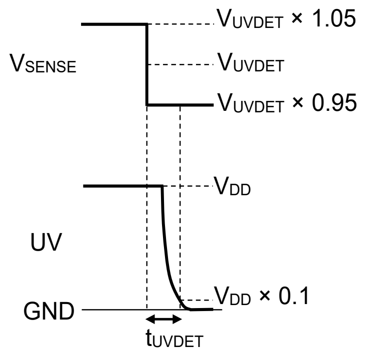
[*2] OV start-up time ($t_{UVSTART}$) is the sum of UVLO release delay time and OV release delay time.

Under Voltage Detection Delay Time (t_{UVDET})

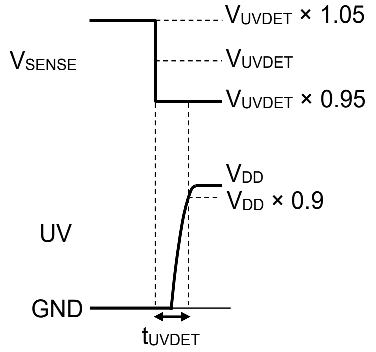
Under voltage detection delay time (t_{UVDET}) means the period from the falling edge of the pulse between V_{UVDET} × 1.05 and V_{UVDET} × 0.95 for SENSE pin to the designated conditions shown below.
NV3601DCxxxA/B: Until UV pin voltage reaches V_{UP} × 0.1. (V_{UP} is pull-up voltage of UV pin)
NV3601DCxxxE/F: Until UV pin voltage reaches V_{DD} × 0.1.
NV3601DCxxxG/H: Until UV pin voltage reaches V_{DD} × 0.9.
As for NV3601DCxxxC/D, the delay time may be longer than expected by the effect of the parasitic capacitance of PCB and pull-up resistor.



NV3601DCxxxA/B



NV3601DCxxxE/F

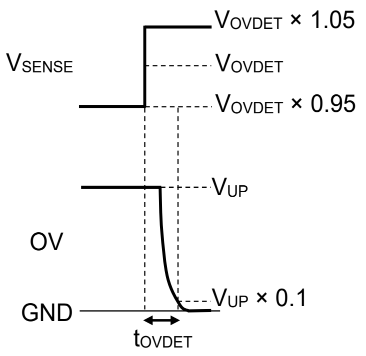


NV3601DCxxxG/H

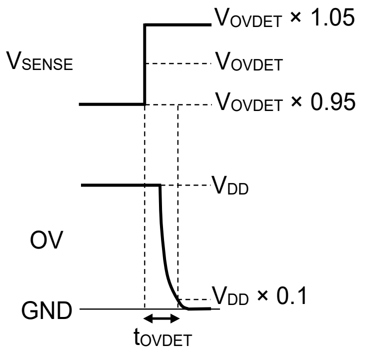
Over Voltage Detection Delay Time (t_{OVDET})

Over voltage detection delay time (t_{OVDET}) means the period from the rising edge of the pulse between V_{OVDET} × 0.95 and V_{OVDET} × 1.05 for SENSE pin to the designated conditions shown below.
NV3601DCxxxA/B: Until OV pin voltage reaches V_{UP} × 0.1. (V_{UP} is pull-up voltage of OV pin)
NV3601DCxxxE/F: Until OV pin voltage reaches V_{DD} × 0.1.
NV3601DCxxxG/H: Until OV pin voltage reaches V_{DD} × 0.9.

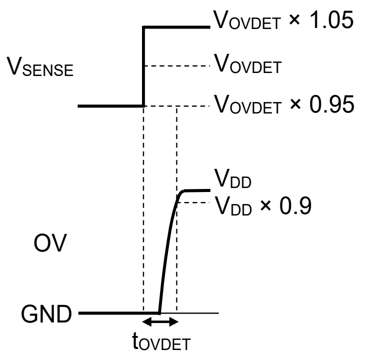
As for NV3601DCxxxC/D, the delay time may be longer than expected by the effect of the parasitic capacitance of PCB and pull-up resistor.



NV3601DCxxxA/B



NV3601DCxxxE/F

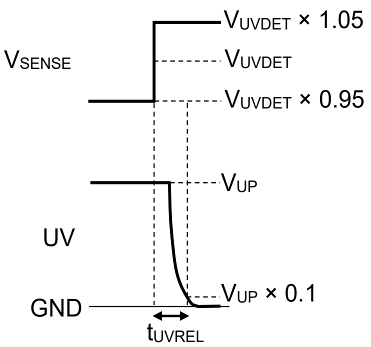


NV3601DCxxxG/H

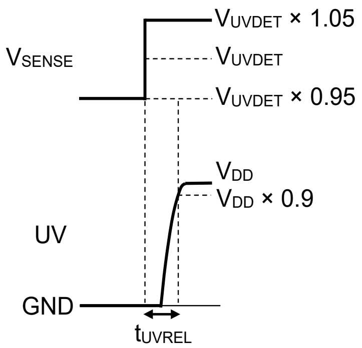
Under Voltage Release Delay Time (t_{UVREL})

Under voltage release delay time (t_{UVREL}) means the period from the rising edge of the pulse between V_{UVDET} × 0.95 and V_{UVDET} × 1.05 to the designated conditions shown below.
NV3601DCxxxC/D: Until UV pin voltage reaches V_{UP} × 0.1. (V_{UP} is pull-up voltage of UV pin.)
NV3601DCxxxE/F: Until UV pin voltage reaches V_{DD} × 0.9.
NV3601DCxxxG/H: Until UV pin voltage reaches V_{DD}× 0.1.

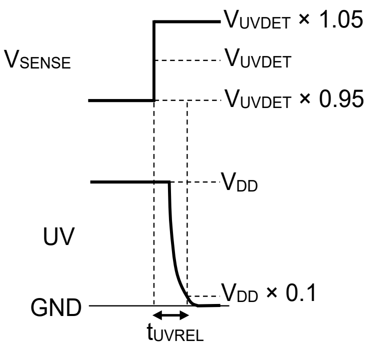
As for NV3601DCxxxA/B, the delay time may be longer than expected by the effect of the parasitic capacitance of PCB and pull-up resistor.



NV3601DCxxxC/D



NV3601DCxxxE/F

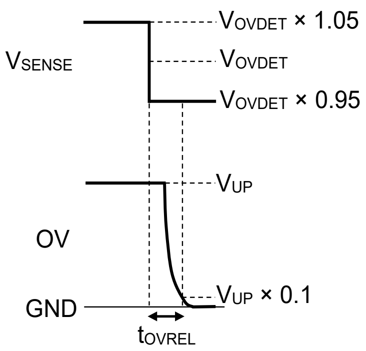


NV3601DCxxxG/H

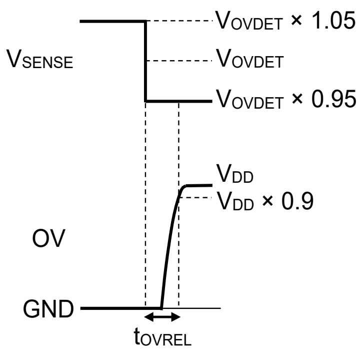
Over Voltage Release Delay Time (t_{OVREL})

Over voltage release delay time (t_{OVREL}) means the period from the falling edge of the pulse between V_{OVDET} × 1.05 and V_{OVDET} × 0.95 for SENSE pin to the designated conditions shown below.
NV3601DCxxxC/D: Until OV pin voltage reaches V_{UP} × 0.1. (V_{UP} is pull-up voltage of OV pin)
NV3601DCxxxE/F: Until OV pin voltage reaches V_{DD} × 0.9.
NV3601DCxxxG/H: Until OV pin voltage reaches V_{DD} × 0.1.

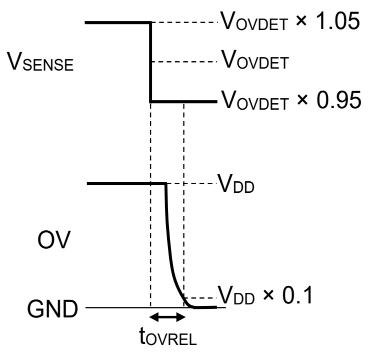
As for NV3601DCxxxA/B, the delay time may be longer than expected by the effect of the parasitic capacitance of PCB and pull-up resistor.



NV3601DCxxxC/D



NV3601DCxxxE/F



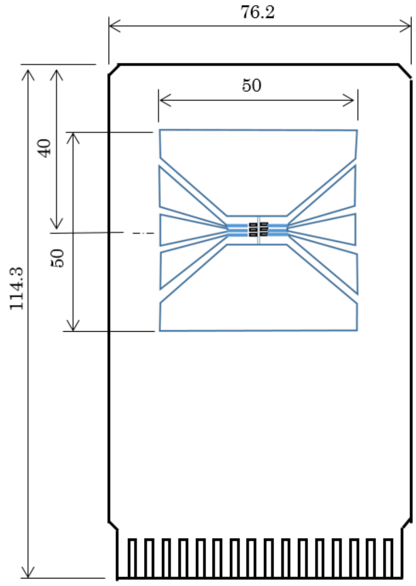
NV3601DCxxxG/H

THERMAL CHARACTERISTICS (SOT-23-DC)

Thermal characteristics depend on the mounting conditions. The following measurement conditions are based on JEDEC STD. 51.

Measurement Conditions

Parameter	Measurement Conditions
Measurement status	Mounting on Board (Wind Velocity = 0 m/s)
Board material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board size	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through hole	ϕ 0.3 mm × 7 pcs



Measurement Board Pattern

Measurement Result

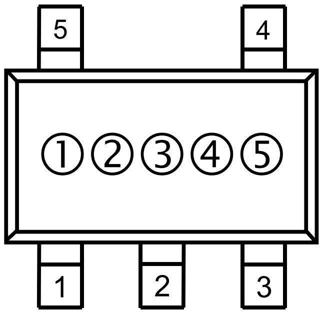
Parameter	Measurement Result
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja : Junction-to-Ambient Thermal Resistance

ψjt : Junction-to-Top Thermal Characterization Parameter

MARKING SPECIFICATION

①②③ : Product Code (Abbreviation)
④⑤ : Lot Number ··· Alphanumeric Serial Number



SOT-23-5-DC Marking

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

Marking List

Product Code	Under Voltage Detection (V_{UVDET}) [V]	Over Voltage Detection (V_{OVDET}) [V]	① ② ③
NV3601DC001A	3.3	4.5	1 0 A
NV3601DC002A	19.8	22.2	1 0 B
NV3601DC003A	9.0	19.7	1 0 C
NV3601DC004A	4.5	18.3	1 0 D
NV3601DC005A	5.7	18.2	1 0 E
NV3601DC006A	8.5	18.5	1 0 F
NV3601DC007A	5.0	19.0	1 0 G
NV3601DC008A	9.7	19.5	1 0 H
NV3601DC009A	8.5	19.5	1 0 J
NV3601DC001B	3.3	4.5	1 1 A
NV3601DC002B	19.8	22.2	1 1 B
NV3601DC003B	9.0	19.7	1 1 C
NV3601DC004B	4.5	18.3	1 1 D
NV3601DC005B	5.7	18.2	1 1 E
NV3601DC006B	8.5	18.5	1 1 F
NV3601DC007B	5.0	19.0	1 1 G
NV3601DC008B	9.7	19.5	1 1 H
NV3601DC009B	8.5	19.5	1 1 J

Marking List

Product Code	Under Voltage Detection (V_{UVDET}) [V]	Over Voltage Detection (V_{OVDET}) [V]	① ② ③
N V 3 6 0 1 D C 0 0 1 C	3.3	4.5	1 2 A
N V 3 6 0 1 D C 0 0 2 C	19.8	22.2	1 2 B
N V 3 6 0 1 D C 0 0 3 C	9.0	19.7	1 2 C
N V 3 6 0 1 D C 0 0 4 C	4.5	18.3	1 2 D
N V 3 6 0 1 D C 0 0 5 C	5.7	18.2	1 2 E
N V 3 6 0 1 D C 0 0 6 C	8.5	18.5	1 2 F
N V 3 6 0 1 D C 0 0 7 C	5.0	19.0	1 2 G
N V 3 6 0 1 D C 0 0 8 C	9.7	19.5	1 2 H
N V 3 6 0 1 D C 0 0 9 C	8.5	19.5	1 2 J
N V 3 6 0 1 D C 0 0 1 D	3.3	4.5	1 3 A
N V 3 6 0 1 D C 0 0 2 D	19.8	22.2	1 3 B
N V 3 6 0 1 D C 0 0 3 D	9.0	19.7	1 3 C
N V 3 6 0 1 D C 0 0 4 D	4.5	18.3	1 3 D
N V 3 6 0 1 D C 0 0 5 D	5.7	18.2	1 3 E
N V 3 6 0 1 D C 0 0 6 D	8.5	18.5	1 3 F
N V 3 6 0 1 D C 0 0 7 D	5.0	19.0	1 3 G
N V 3 6 0 1 D C 0 0 8 D	9.7	19.5	1 3 H
N V 3 6 0 1 D C 0 0 9 D	8.5	19.5	1 3 J
N V 3 6 0 1 D C 0 0 1 E	3.3	4.5	1 4 A
N V 3 6 0 1 D C 0 0 2 E	19.8	22.2	1 4 B
N V 3 6 0 1 D C 0 0 3 E	9.0	19.7	1 4 C
N V 3 6 0 1 D C 0 0 4 E	4.5	18.3	1 4 D
N V 3 6 0 1 D C 0 0 5 E	5.7	18.2	1 4 E
N V 3 6 0 1 D C 0 0 6 E	8.5	18.5	1 4 F
N V 3 6 0 1 D C 0 0 7 E	5.0	19.0	1 4 G
N V 3 6 0 1 D C 0 0 8 E	9.7	19.5	1 4 H
N V 3 6 0 1 D C 0 0 9 E	8.5	19.5	1 4 J
N V 3 6 0 1 D C 0 0 1 F	3.3	4.5	1 5 A
N V 3 6 0 1 D C 0 0 2 F	19.8	22.2	1 5 B
N V 3 6 0 1 D C 0 0 3 F	9.0	19.7	1 5 C
N V 3 6 0 1 D C 0 0 4 F	4.5	18.3	1 5 D
N V 3 6 0 1 D C 0 0 5 F	5.7	18.2	1 5 E
N V 3 6 0 1 D C 0 0 6 F	8.5	18.5	1 5 F
N V 3 6 0 1 D C 0 0 7 F	5.0	19.0	1 5 G
N V 3 6 0 1 D C 0 0 8 F	9.7	19.5	1 5 H
N V 3 6 0 1 D C 0 0 9 F	8.5	19.5	1 5 J

Marking List

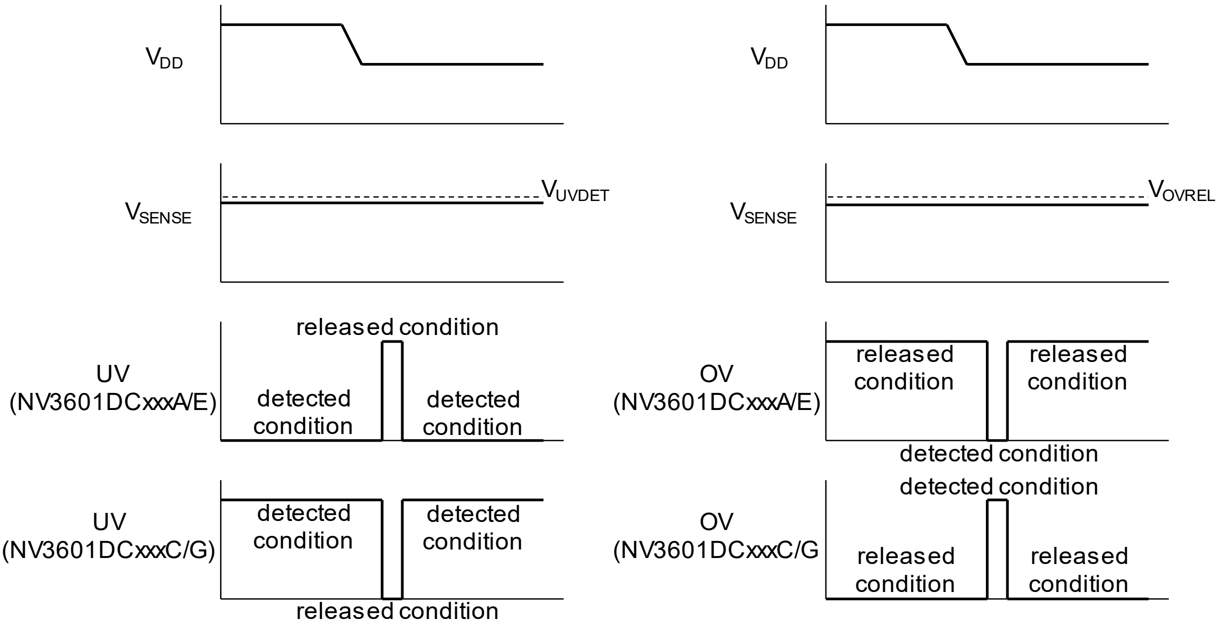
Product Code	Under Voltage Detection (V_{UVDET}) [V]	Over Voltage Detection (V_{OVDET}) [V]	① ② ③
N V 3 6 0 1 D C 0 0 1 G	3.3	4.5	1 6 A
N V 3 6 0 1 D C 0 0 2 G	19.8	22.2	1 6 B
N V 3 6 0 1 D C 0 0 3 G	9.0	19.7	1 6 C
N V 3 6 0 1 D C 0 0 4 G	4.5	18.3	1 6 D
N V 3 6 0 1 D C 0 0 5 G	5.7	18.2	1 6 E
N V 3 6 0 1 D C 0 0 6 G	8.5	18.5	1 6 F
N V 3 6 0 1 D C 0 0 7 G	5.0	19.0	1 6 G
N V 3 6 0 1 D C 0 0 8 G	9.7	19.5	1 6 H
N V 3 6 0 1 D C 0 0 9 G	8.5	19.5	1 6 J
N V 3 6 0 1 D C 0 0 1 H	3.3	4.5	1 7 A
N V 3 6 0 1 D C 0 0 2 H	19.8	22.2	1 7 B
N V 3 6 0 1 D C 0 0 3 H	9.0	19.7	1 7 C
N V 3 6 0 1 D C 0 0 4 H	4.5	18.3	1 7 D
N V 3 6 0 1 D C 0 0 5 H	5.7	18.2	1 7 E
N V 3 6 0 1 D C 0 0 6 H	8.5	18.5	1 7 F
N V 3 6 0 1 D C 0 0 7 H	5.0	19.0	1 7 G
N V 3 6 0 1 D C 0 0 8 H	9.7	19.5	1 7 H
N V 3 6 0 1 D C 0 0 9 H	8.5	19.5	1 7 J

APPLICATIONS NOTES

Power-up Considerations
When SENSE pin voltage (V_{SENSE}) is in between UV detection voltage and release voltage, OV detection voltage and release voltage, output voltage may indefinite depending on the slew rate of VDD pin voltage (V_{DD}) and rising level width.

Power-down Considerations
As for NV3601DCxxxA/C/E/G, when SENSE pin voltage (V_{SENSE}) is just a little lower than the under voltage detection voltage (V_{UVDET}), if VDD pin voltage (V_{DD}) goes down drastically, UV pin may release a pulse shown the below figure. When V_{SENSE} is just a little lower than the over voltage release voltage (V_{OVREL}), if V_{DD} goes down drastically, OV pin may release a pulse shown the below figure. In such cases, put a capacitor (C_{IN}) between VDD pin and GND pin to make falling speed of V_{DD} slow.
In the case of $V_{SENSE} = V_{UVDET} \times 0.99$, or $V_{SENSE} = V_{OVREL} \times 0.985$, we recommend the falling slew rate of V_{DD} is slower than -10 mV/µs.

As for NV3601DCxxxB/D/F/H, there is no hysteresis voltage, therefore, the impact from the power fluctuation may be serious. If the extra capacitor between VDD pin and GND pin is not effective, add another capacitor between UV/OV pins and GND.



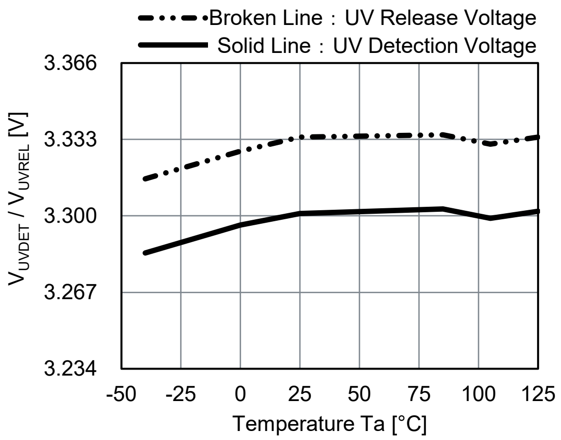
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.
V_{DD} = 3.3 V, NV3601DCxxxE, Ta = 25 °C unless otherwise noted.

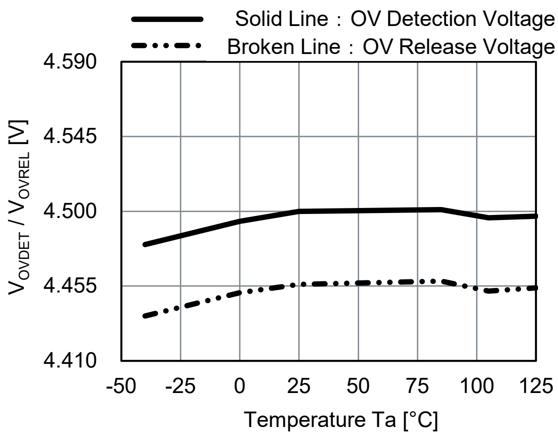
1) UV Detection / Release Voltage vs Temperature

OV Detection / Release Voltage vs Temperature

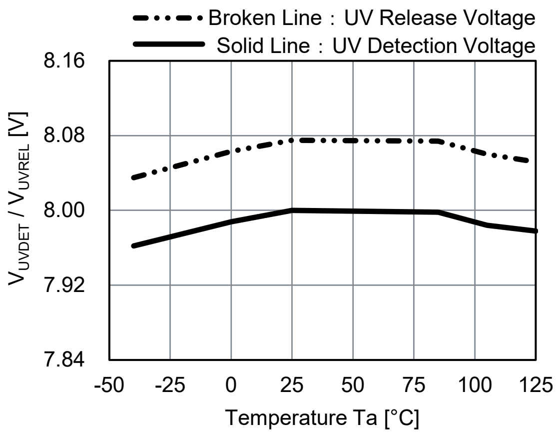
V_{UVDET} = 3.3 V



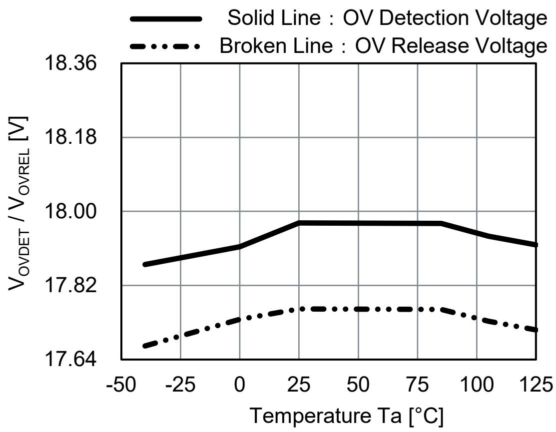
V_{OVDET} = 4.5 V



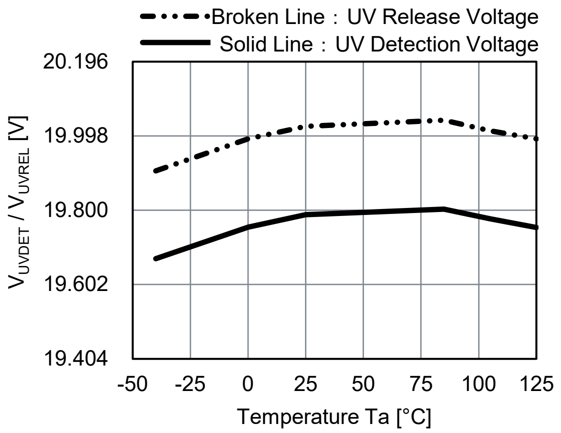
V_{UVDET} = 8.0 V



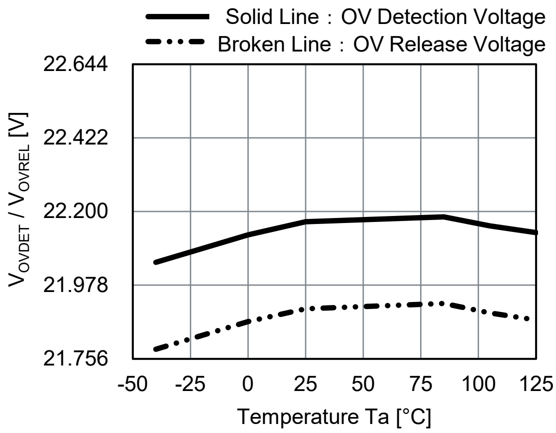
V_{OVDET} = 18.0 V



V_{UVDET} = 19.8 V

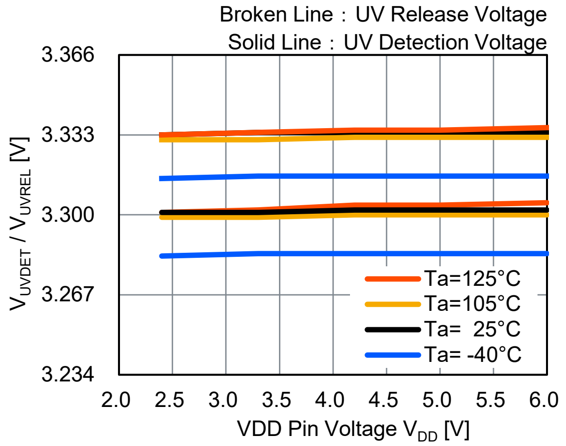


V_{OVDET} = 22.2 V



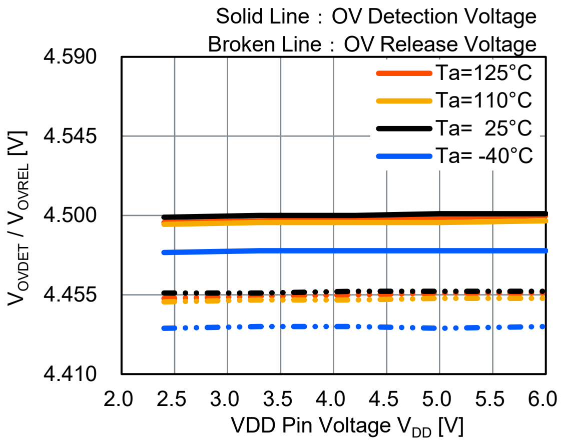
2) UV Detection / Release Voltage vs VDD Pin Voltage

V_{UVDET} = 3.3 V

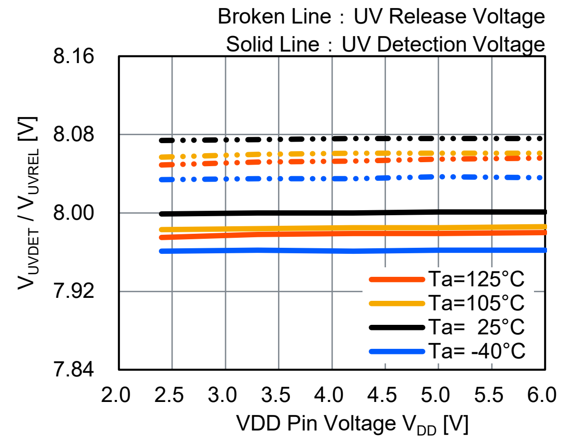


OV Detection / Release Voltage vs VDD Pin Voltage

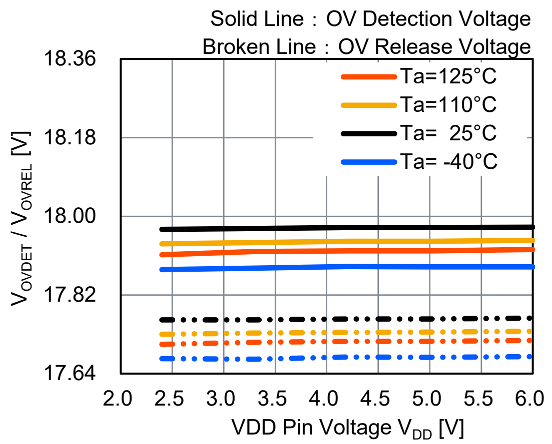
V_{OVDET} = 4.5 V



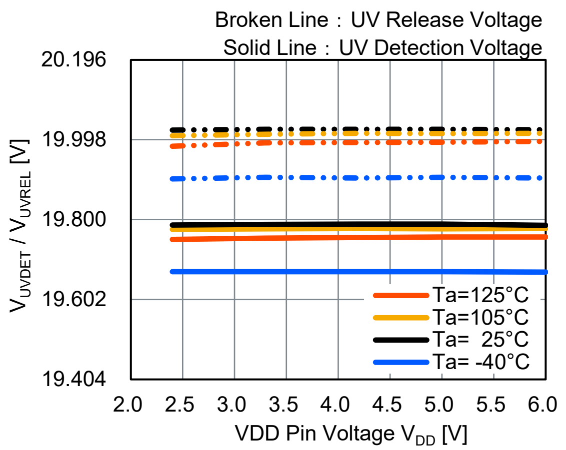
V_{UVDET} = 8.0 V



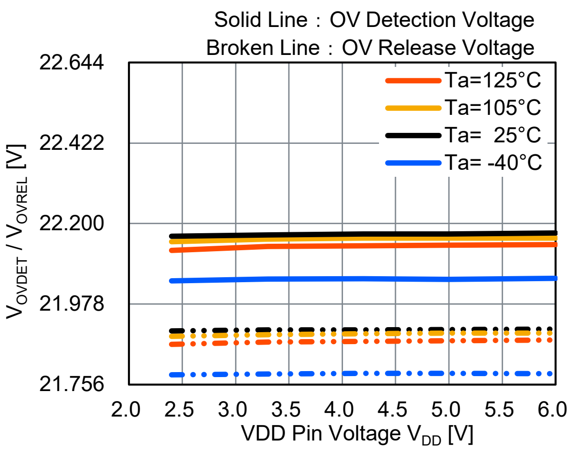
V_{OVDET} = 18.0 V



V_{UVDET} = 19.8 V

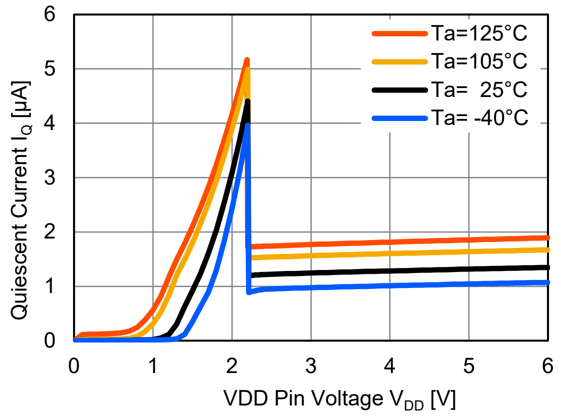


V_{OVDET} = 22.2 V



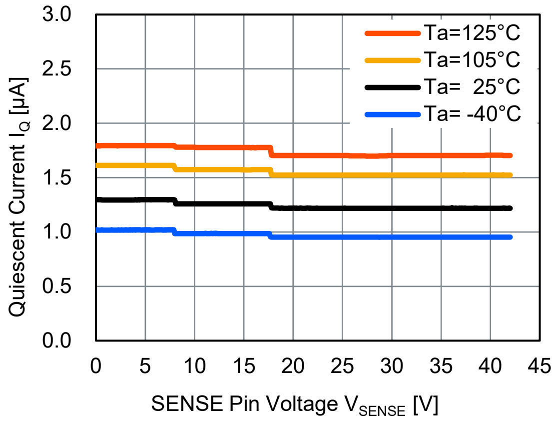
3) Quiescent Current vs VDD Pin Voltage

V_{UVDET} = 8.0 V, V_{OVDET} = 18.0 V, V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2
V_{DD} = 6.0 V to 0 V



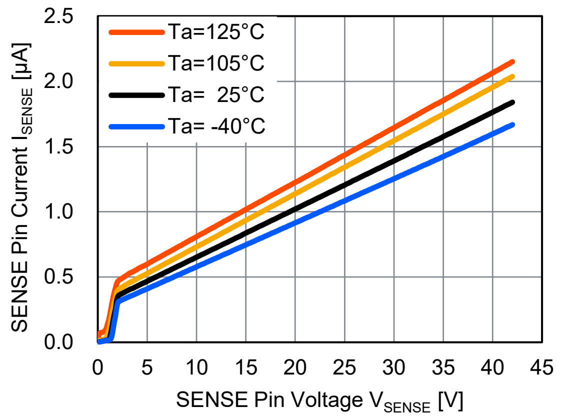
4) Quiescent Current vs SENSE Pin Voltage

V_{UVDET} = 8.0 V, V_{OVDET} = 18.0 V

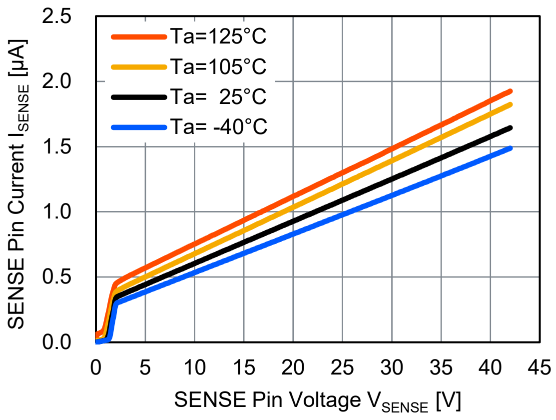


5) SENSE Pin Current vs SENSE Pin Voltage

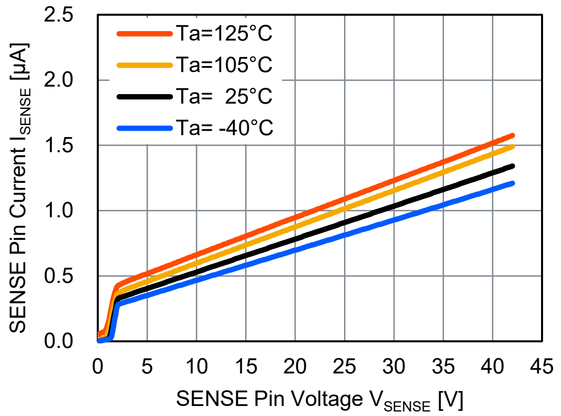
V_{UVDET} = 3.3 V, V_{OVDET} = 4.5 V



V_{UVDET} = 8.0 V, V_{OVDET} = 18.0 V



V_{UVDET} = 19.8 V, V_{OVDET} = 22.2 V

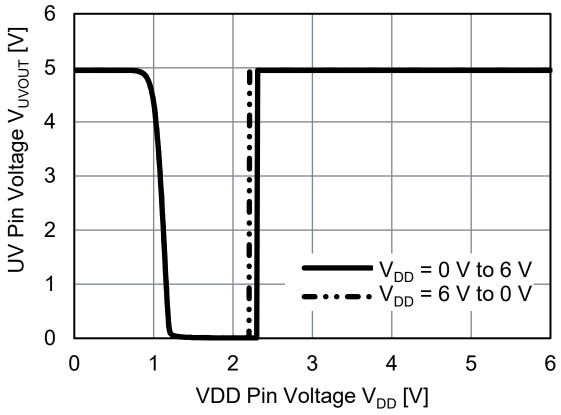


6) UV Pin Voltage vs VDD Pin Voltage

NV3601DCxxxA

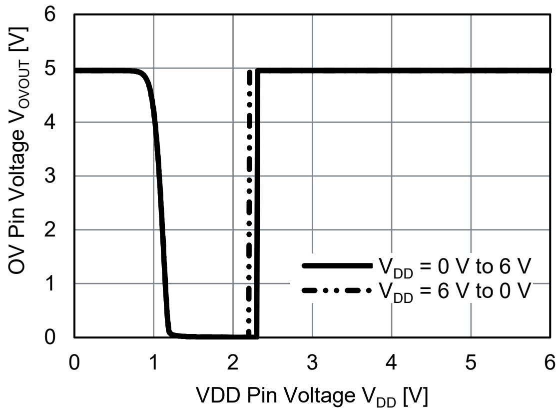
$V_{UVUP} = V_{OVUP} = 5.0$ V, $R_{UP} = 100$ kΩ

$V_{UVDET} = 8.0$ V, $V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2$



OV Pin Voltage vs VDD Pin Voltage

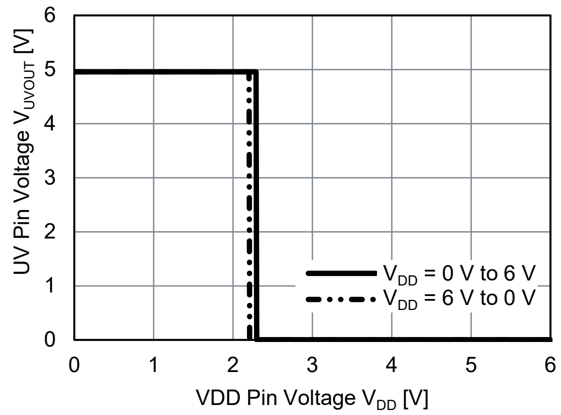
$V_{OVDET} = 18.0$ V, $V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2$



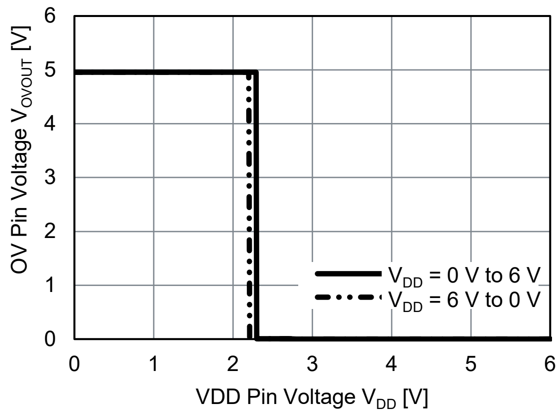
NV3601DCxxxC

$V_{UVUP} = V_{OVUP} = 5.0$ V, $R_{UP} = 100$ kΩ

$V_{UVDET} = 8.0$ V, $V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2$

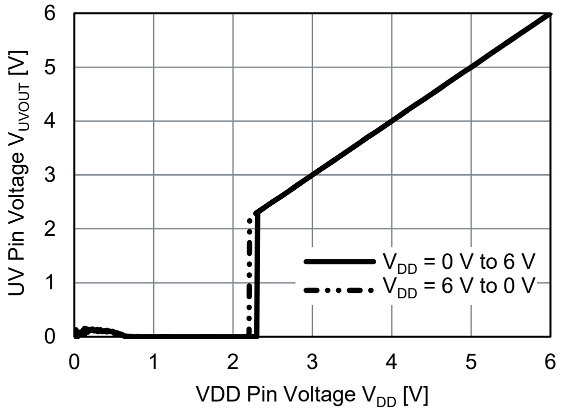


$V_{OVDET} = 18.0$ V, $V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2$

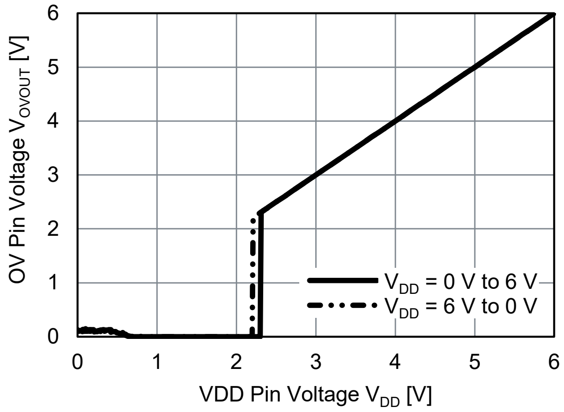


NV3601DCxxxE

V_{UVDET} = 8.0 V, V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2

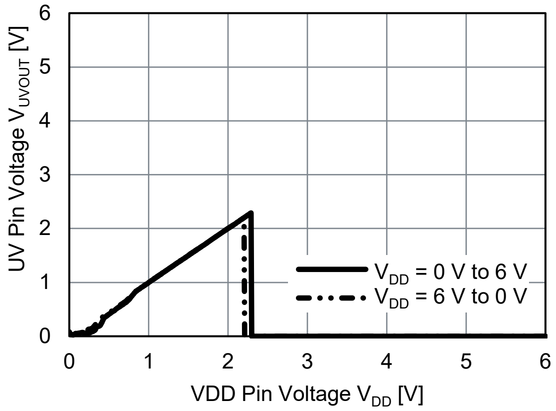


V_{OVDET} = 18.0 V, V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2

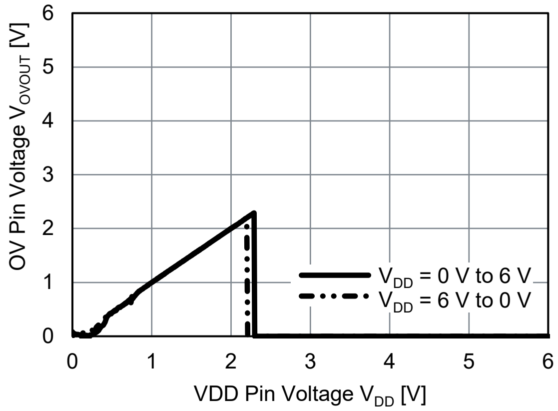


NV3601DCxxxG

V_{UVDET} = 8.0 V, V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2



V_{OVDET} = 18.0 V, V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2

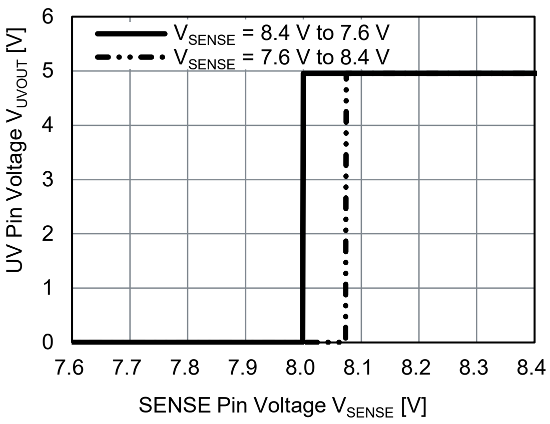


7) UV Pin Voltage vs SENSE Pin Voltage

NV3601DCxxxA

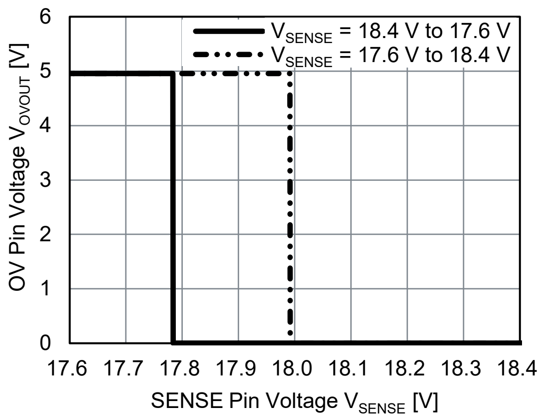
$V_{UVUP} = V_{OVUP} = 5.0$ V, $R_{UP} = 100$ kΩ

$V_{UVDET} = 8.0$ V



OV Pin Voltage vs SENSE Pin Voltage

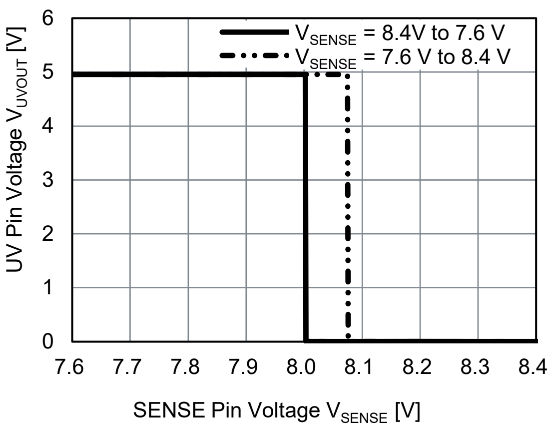
$V_{OVDET} = 18.0$ V



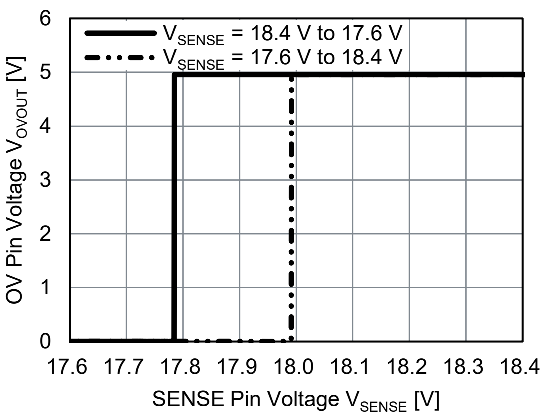
NV3601DCxxxC

$V_{UVUP} = V_{OVUP} = 5.0$ V, $R_{UP} = 100$ kΩ

$V_{UVDET} = 8.0$ V

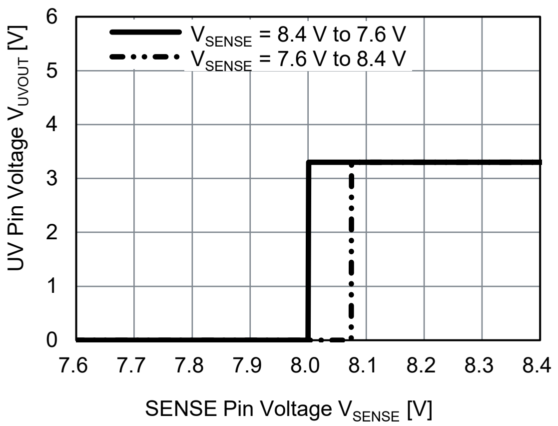


$V_{OVDET} = 18.0$ V

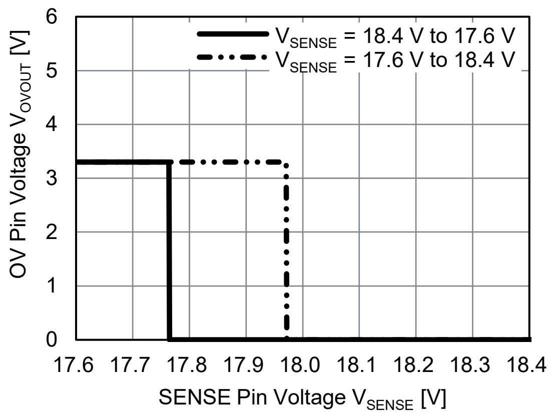


NV3601DCxxxE

V_{UVDET} = 8.0 V

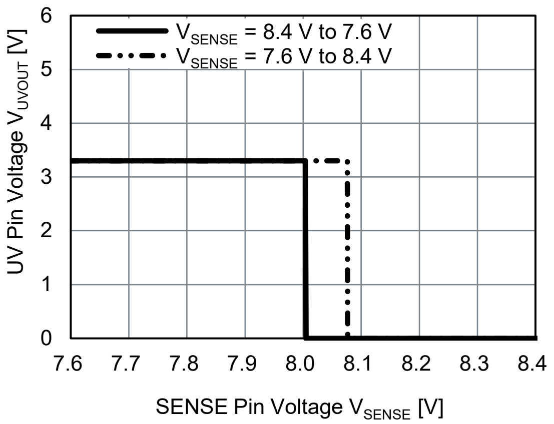


V_{OVDET} = 18.0 V

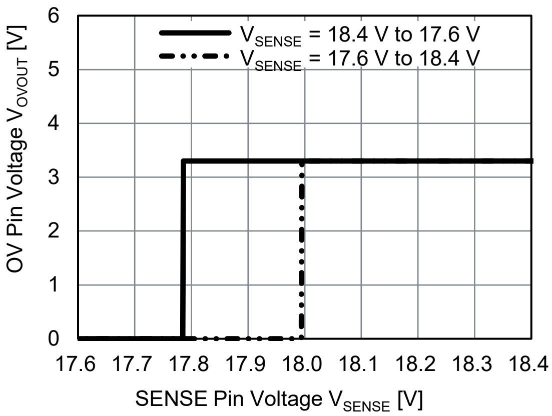


NV3601DCxxxG

V_{UVDET} = 8.0 V

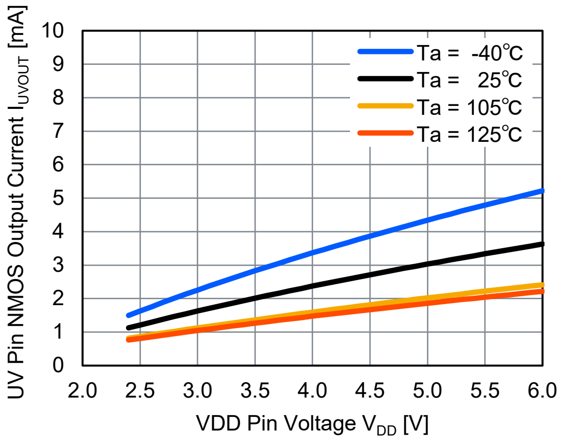


V_{OVDET} = 18.0 V



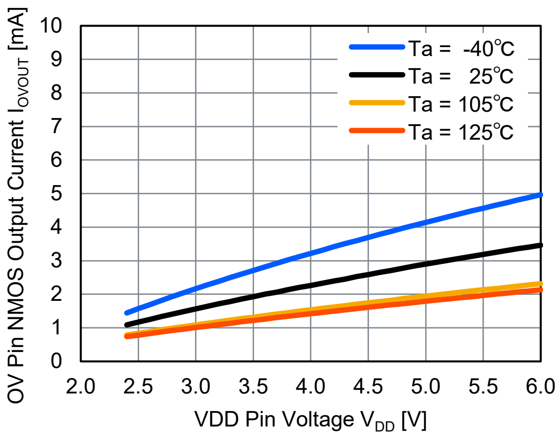
8) UV Pin NMOS Output Current vs VDD Pin Voltage

V_{UVDET} = 8.0 V, V_{SENSE} = 0 V, V_{UVOUT} = 0.1 V



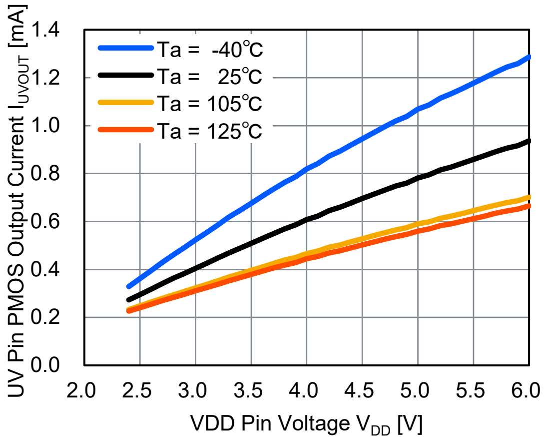
OV Pin NMOS Output Current vs VDD Pin Voltage

V_{OVDET} = 18.0 V, V_{SENSE} = 24 V, V_{OVOUT} = 0.1 V



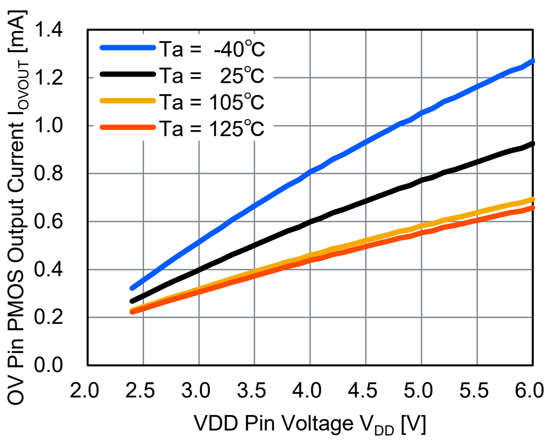
9) UV Pin PMOS Output Current vs VDD Pin Voltage

V_{UVDET} = 8.0 V, V_{SENSE} = 24 V, V_{UVOUT} = V_{DD} - 0.1 V

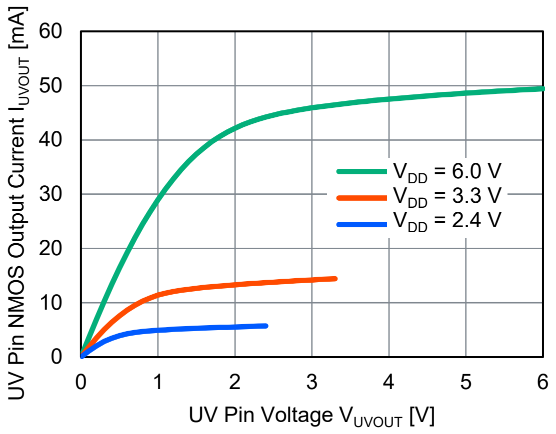


OV Pin PMOS Output Current vs VDD Pin Voltage

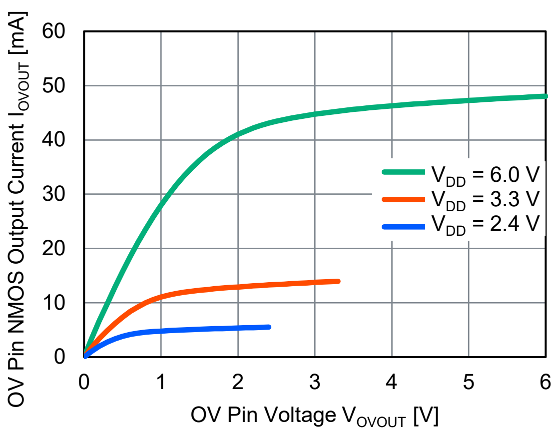
V_{OVDET} = 18.0 V, V_{SENSE} = 0 V, V_{OVOUT} = V_{DD} - 0.1 V



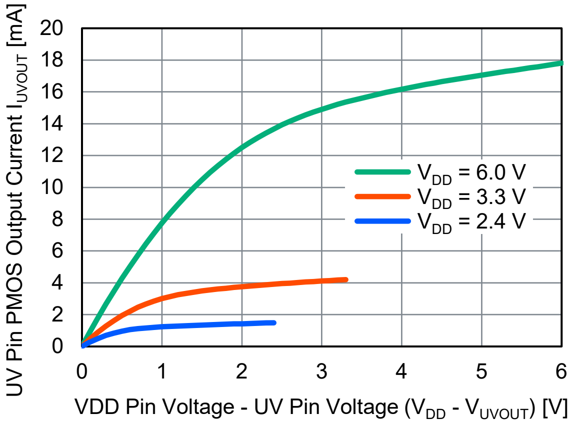
10) UV Pin NMOS Output Current vs UV Pin Voltage
V_{UVDET} = 8.0 V, V_{SENSE} = 0 V, V_{UVOUT} = 0 V to V_{DD}



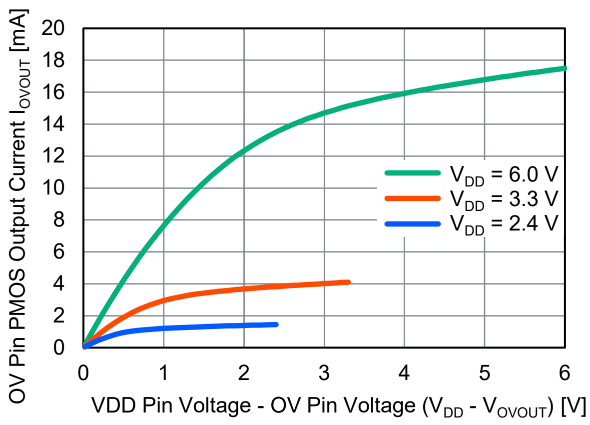
OV Pin NMOS Output Current vs OV Pin Voltage
V_{OVDET} = 18.0 V, V_{SENSE} = 24 V, V_{OVOUT} = 0 V to V_{DD}



11) UV Pin PMOS Output Current
vs VDD Pin Voltage - UV Pin Voltage
V_{UVDET} = 8.0 V, V_{SENSE} = 24 V, V_{UVOUT} = V_{DD} to 0 V

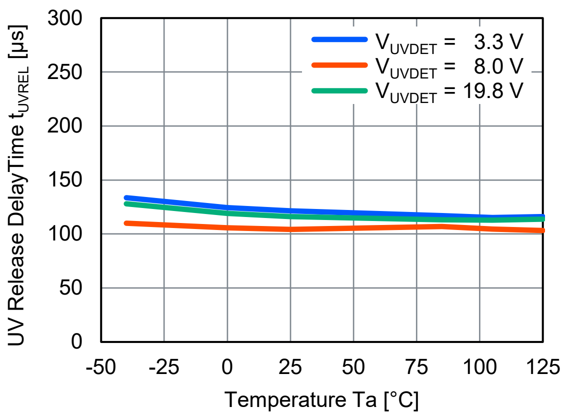


OV Pin PMOS Output Current
vs VDD Pin Voltage - OV Pin Voltage
V_{OVDET} = 18.0 V, V_{SENSE} = 0 V, V_{OVOUT} = V_{DD} to 0 V



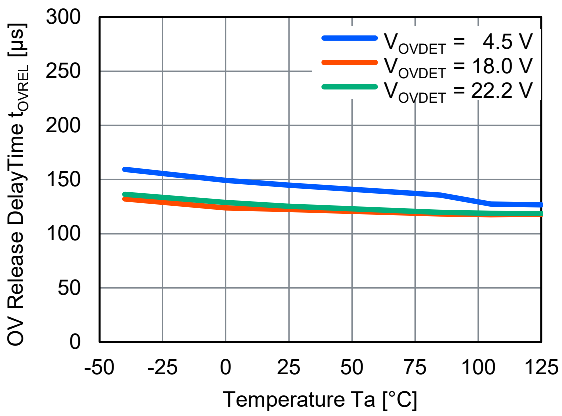
12) UV Release Delay Time vs Temperature

$V_{SENSE} = V_{UVDET} \times 0.95$ to $V_{UVDET} \times 1.05$



OV Release Delay Time vs Temperature

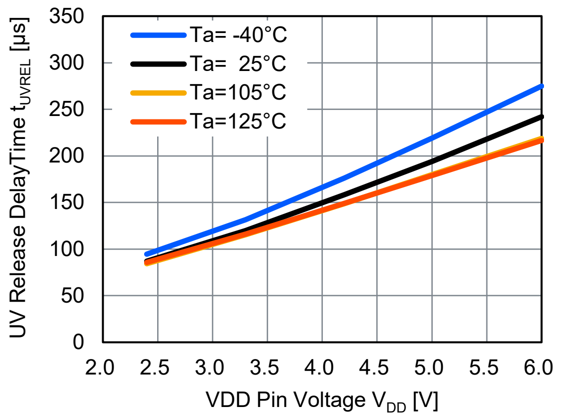
$V_{SENSE} = V_{OVDET} \times 1.05$ to $V_{OVDET} \times 0.95$



13) UV Release Delay Time vs VDD Pin Voltage

$V_{SENSE} = V_{UVDET} \times 0.95$ to $V_{UVDET} \times 1.05$

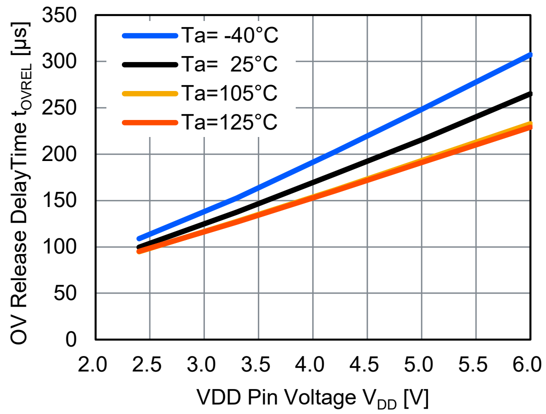
$V_{UVDET} = 3.3$ V



OV Release Delay Time vs VDD Pin Voltage

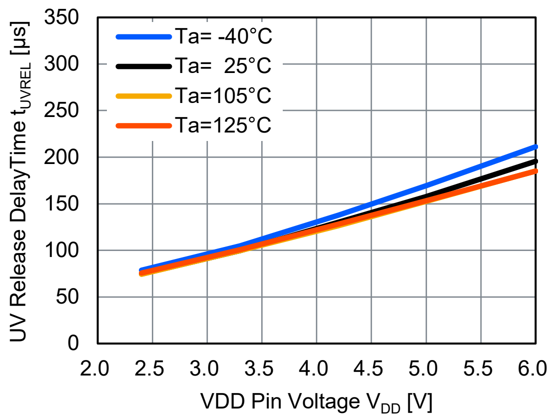
$V_{SENSE} = V_{OVDET} \times 1.05$ to $V_{OVDET} \times 0.95$

$V_{OVDET} = 4.5$ V



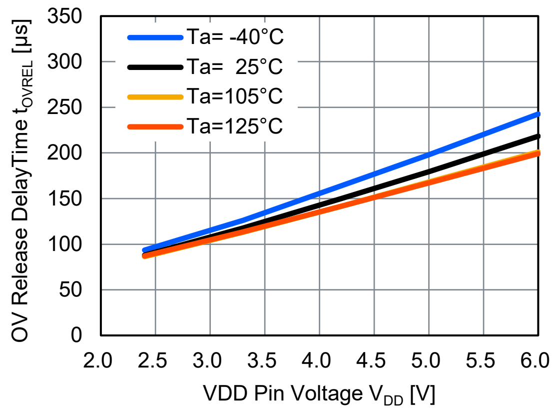
$V_{SENSE} = V_{UVDET} \times 0.95$ to $V_{UVDET} \times 1.05$

$V_{UVDET} = 8.0$ V

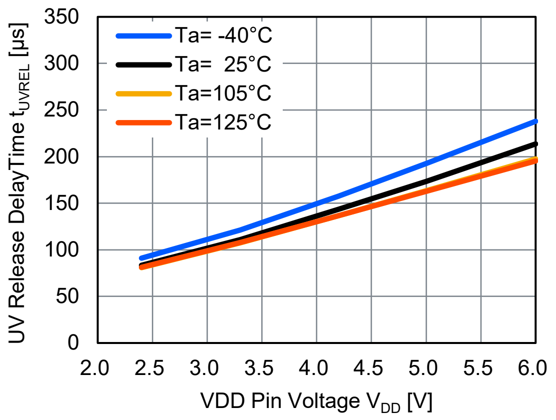


$V_{SENSE} = V_{OVDET} \times 1.05$ to $V_{OVDET} \times 0.95$

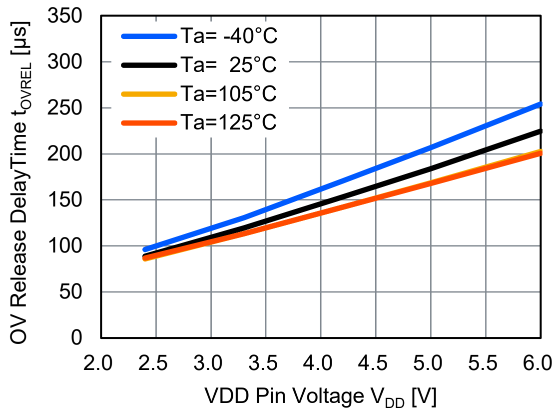
$V_{OVDET} = 18.0$ V



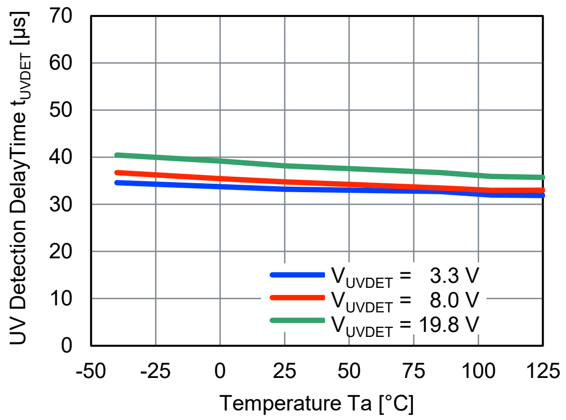
$V_{SENSE} = V_{UVDET} \times 0.95$ to $V_{UVDET} \times 1.05$
$V_{UVDET} = 19.8V$



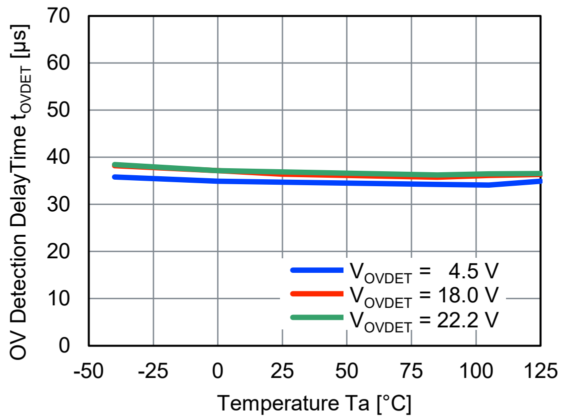
$V_{SENSE} = V_{OVDET} \times 1.05$ to $V_{OVDET} \times 0.95$
$V_{OVDET} = 22.2$ V



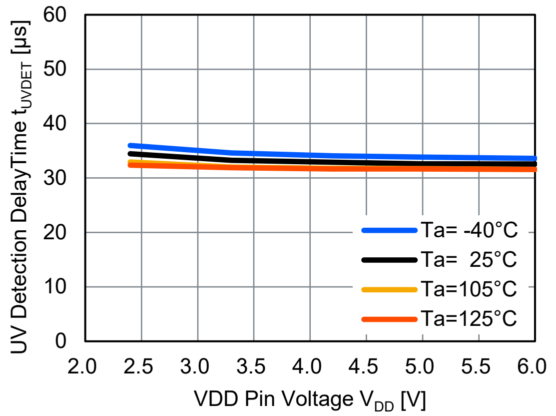
14) UV Detection Delay Time vs Temperature
$V_{SENSE} = V_{UVDET} \times 1.05$ to $V_{UVDET} \times 0.95$



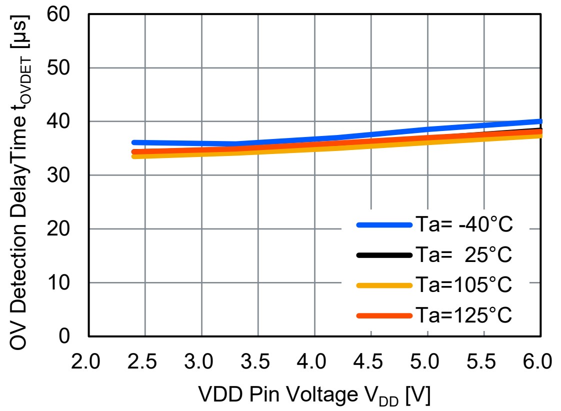
OV Detection Delay Time vs Temperature
$V_{SENSE} = V_{OVDET} \times 0.95$ to $V_{OVDET} \times 1.05$



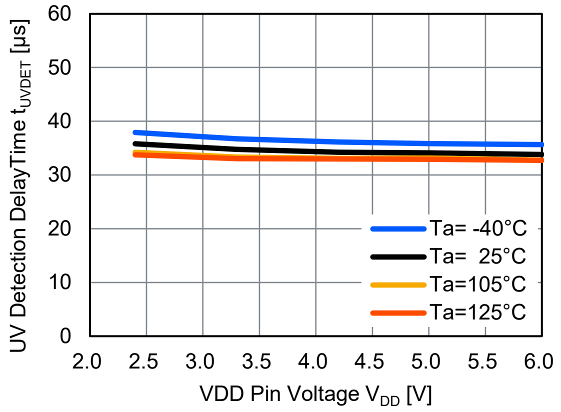
15) UV Detection Delay Time vs VDD Pin Voltage
$V_{SENSE} = V_{UVDET} \times 1.05$ to $V_{UVDET} \times 0.95$
$V_{UVDET} = 3.3$ V



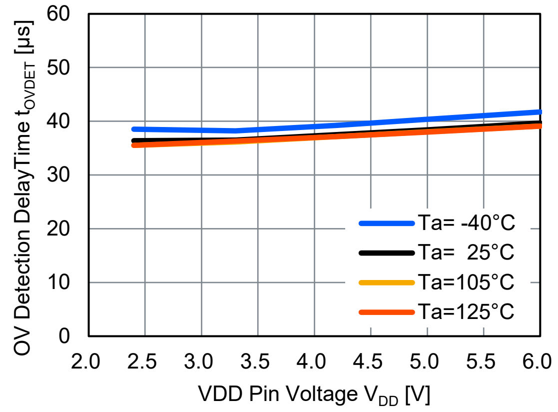
OV Detection Delay Time vs VDD Pin Voltage
$V_{SENSE} = V_{OVDET} \times 0.95$ to $V_{OVDET} \times 1.05$
$V_{OVDET} = 4.5$ V



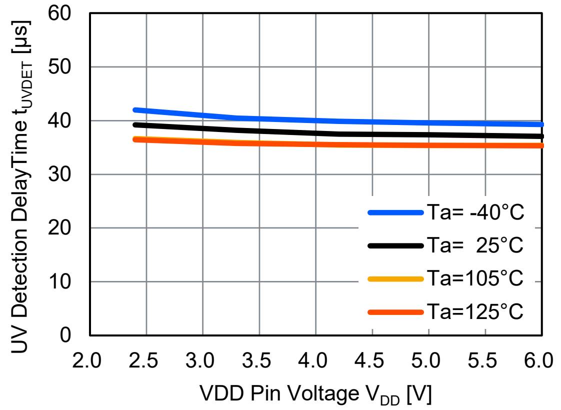
V_{SENSE} = V_{UVDET} × 1.05 to V_{UVDET} × 0.95
V_{UVDET} = 8.0 V



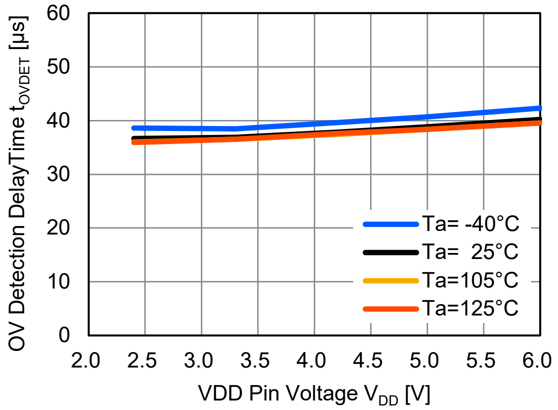
V_{SENSE} = V_{OVDET} × 0.95 to V_{OVDET} × 1.05
V_{OVDET} = 18.0 V



V_{SENSE} = V_{UVDET} × 1.05 to V_{UVDET} × 0.95
V_{UVDET} = 19.8 V



V_{SENSE} = V_{OVDET} × 0.95 to V_{OVDET} × 1.05
V_{OVDET} = 22.2 V

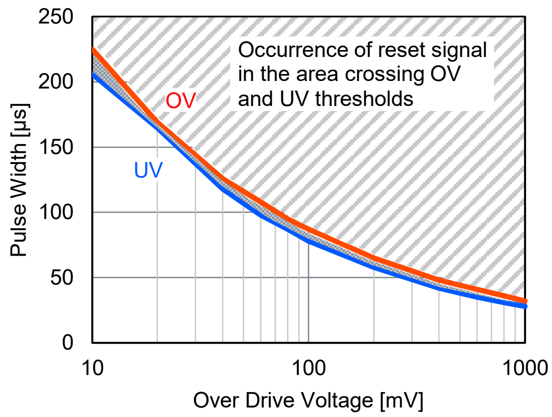


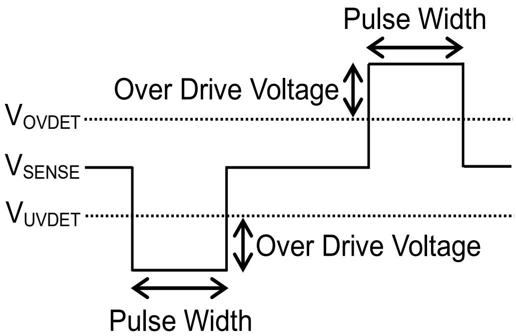
16) SENSE Pin Pulse Width vs Over Drive Voltage

$V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2 \Leftrightarrow V_{UVDET}$ - Over Drive Voltage

$V_{SENSE} = (V_{UVDET} + V_{OVDET}) / 2 \Leftrightarrow V_{OVDET}$ + Over Drive Voltage

$V_{UVDET} = 8.0$ V, $V_{OVDET} = 18.0$ V



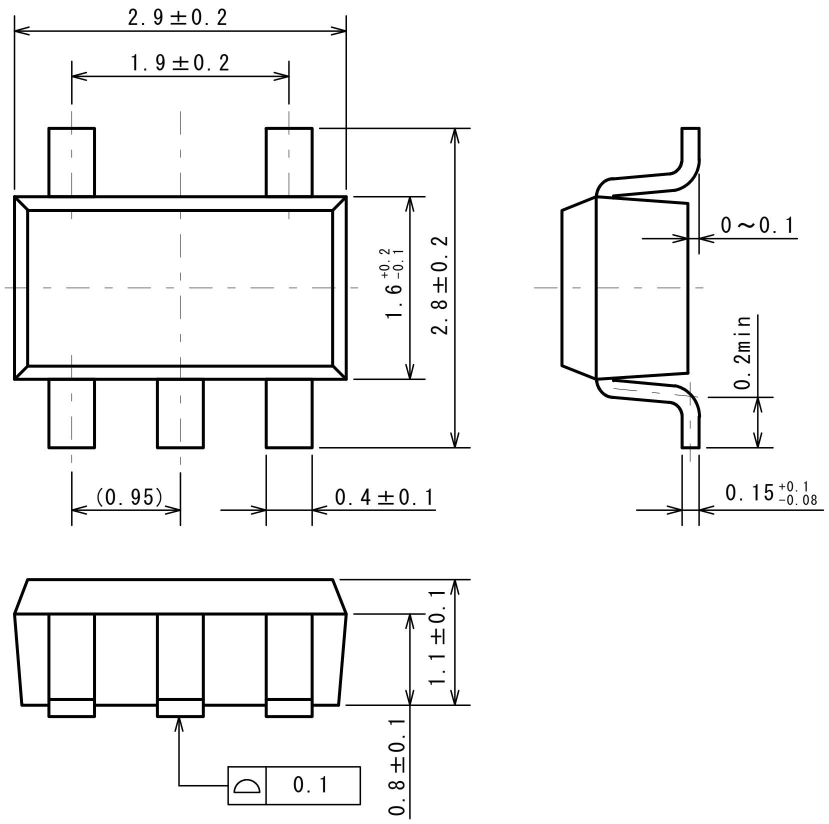


Nisshinbo Micro Devices Inc.

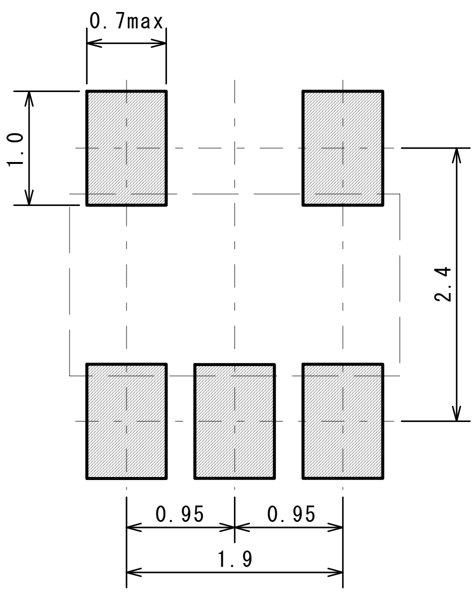
SOT-23-5-DC

■ PACKAGE DIMENSIONS

UNIT: mm



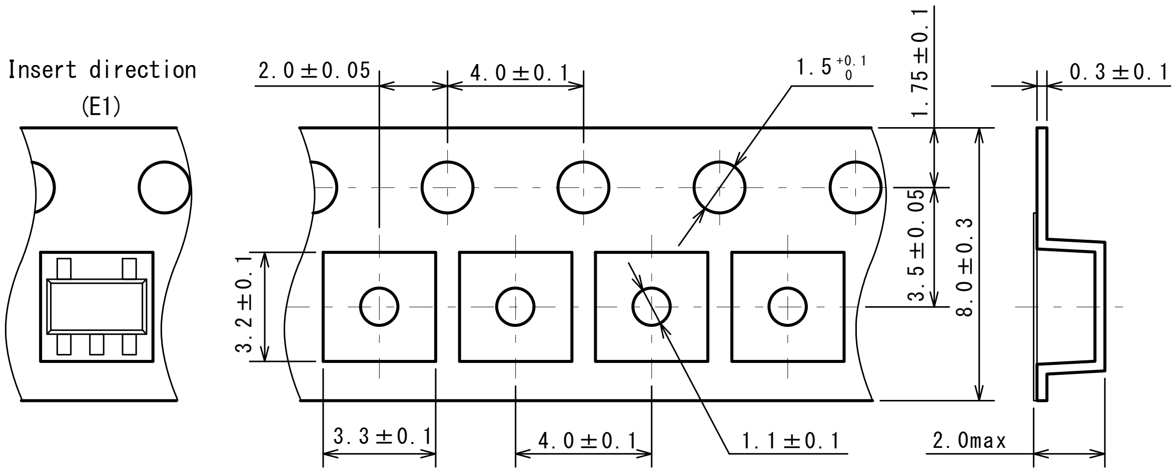
■ EXAMPLE OF SOLDER PADS DIMENSIONS



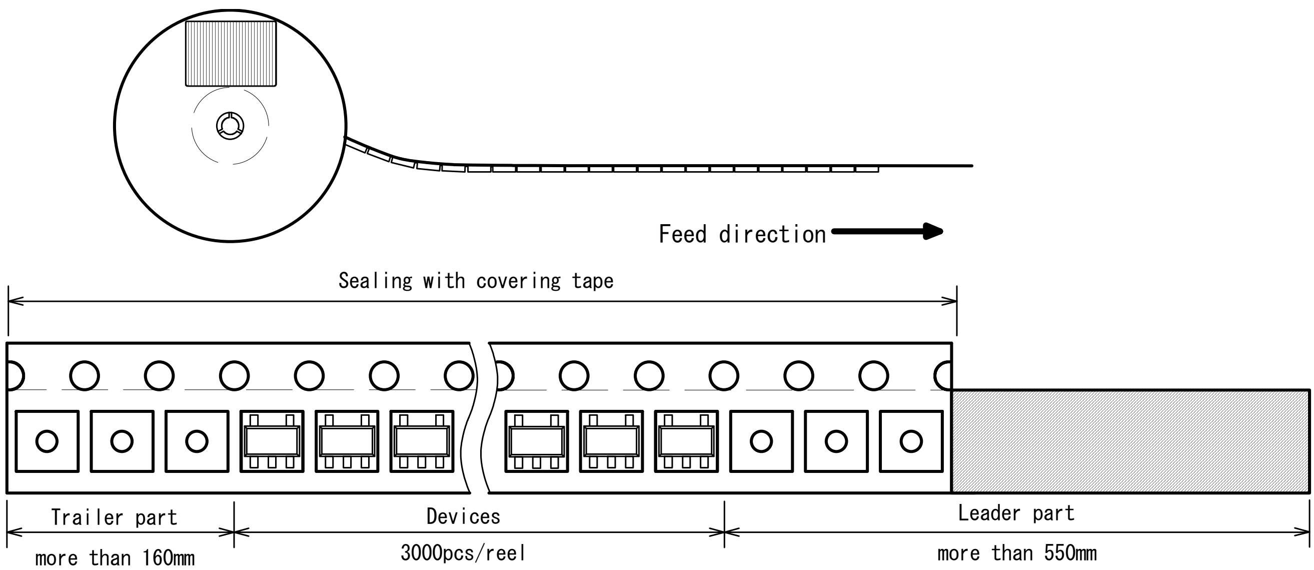
■ PACKING SPEC

UNIT: mm

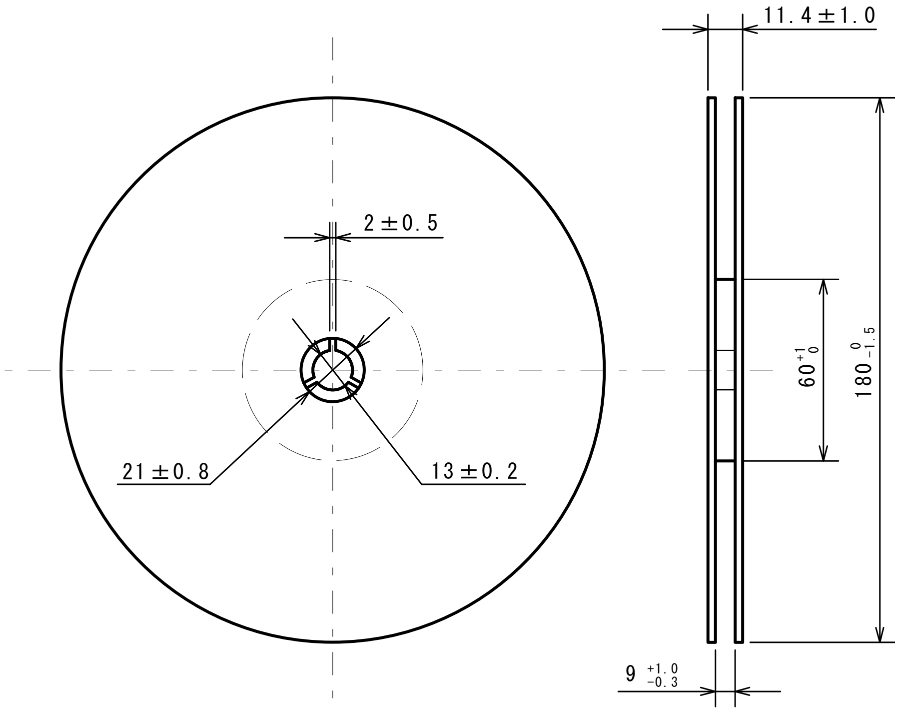
(1) Taping dimensions / Insert direction



(2) Taping state



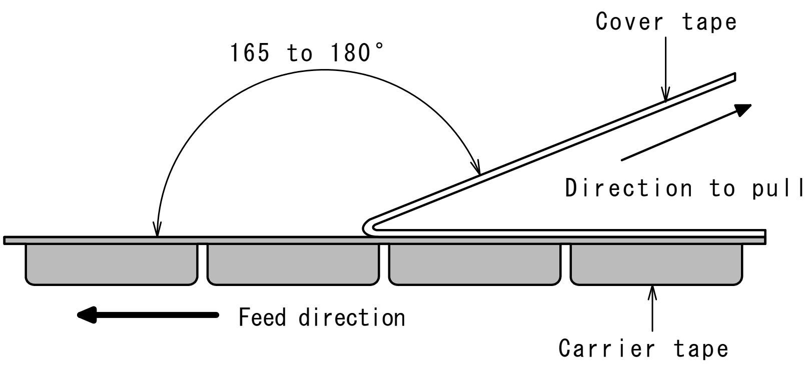
(3) Reel dimensions



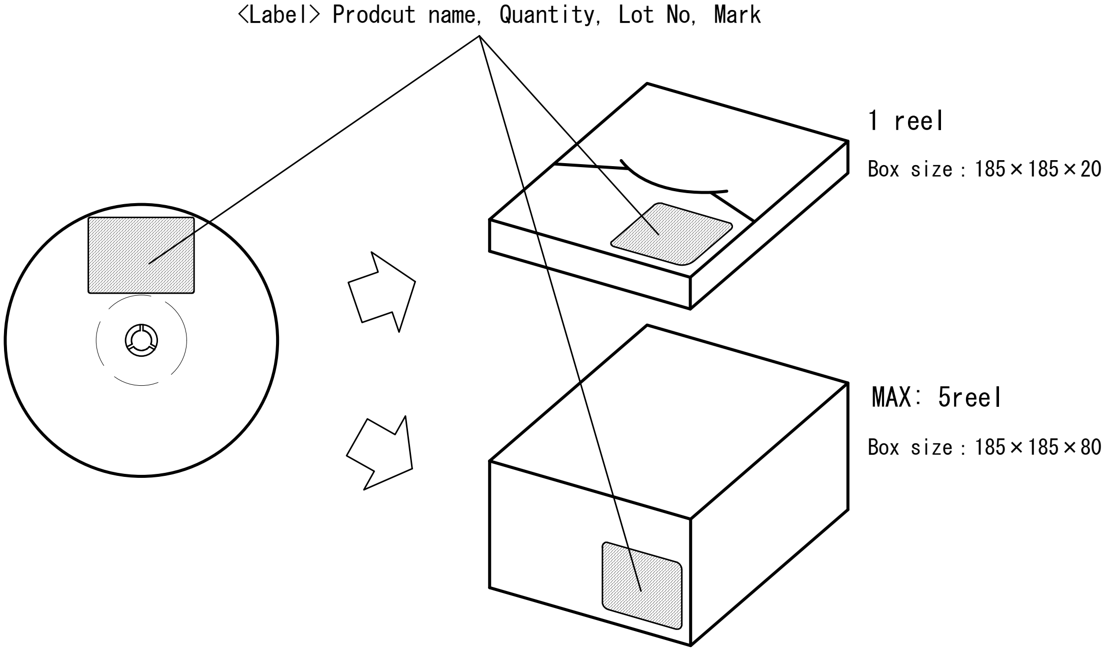
(4) Peeling strength

Peeling strength of cover tape

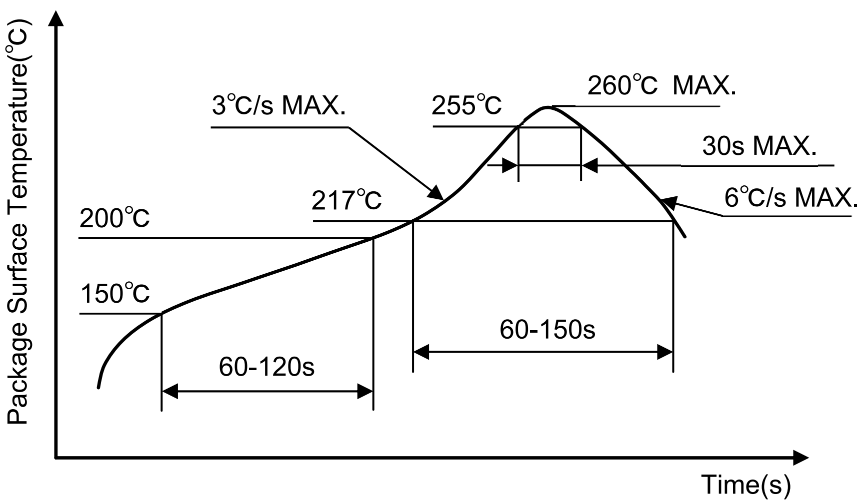
- ･Peeling angle 165 to 180° degrees to the taped surface.
- ･Peeling speed 300mm/min
- ･Peeling strength 0.1 to 1.0N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

REVISION HISTORY

Date	Revision	Contents of Changes
September 08, 2023	1.0	Initial release

NISSHINBO

Nisshinbo Micro Devices Inc.

Official website
https://www.nisshinbo-microdevices.co.jp/en/

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